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(54) **SEMICONDUCTOR AND OPTOELECTRONIC DEVICES**

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CPC ***H01L 27/14605*** (2013.01); ***H01L 27/14612*** (2013.01); *H01L 21/8221* (2013.01); *H01L 27/14634* (2013.01)

(58) **Field of Classification Search**
CPC H01L 27/14612; H01L 27/14634; H01L 21/8221
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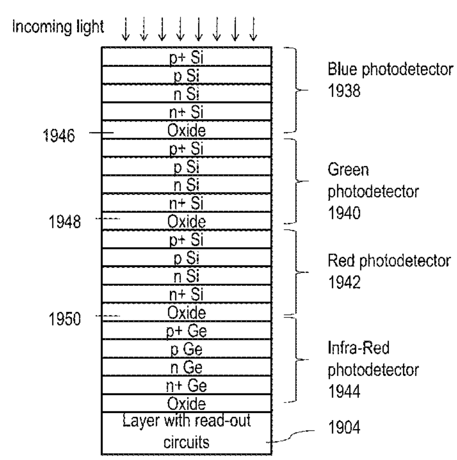
(57) **ABSTRACT**

An integrated device, including: a first mono-crystal layer including a plurality of image sensor pixels and alignment marks; an overlaying oxide on top of the first mono-crystal layer; and a second mono-crystal layer overlaying the oxide, where the second mono-crystal layer includes a plurality of single crystal transistors aligned to the alignment marks.

20 Claims, 147 Drawing Sheets



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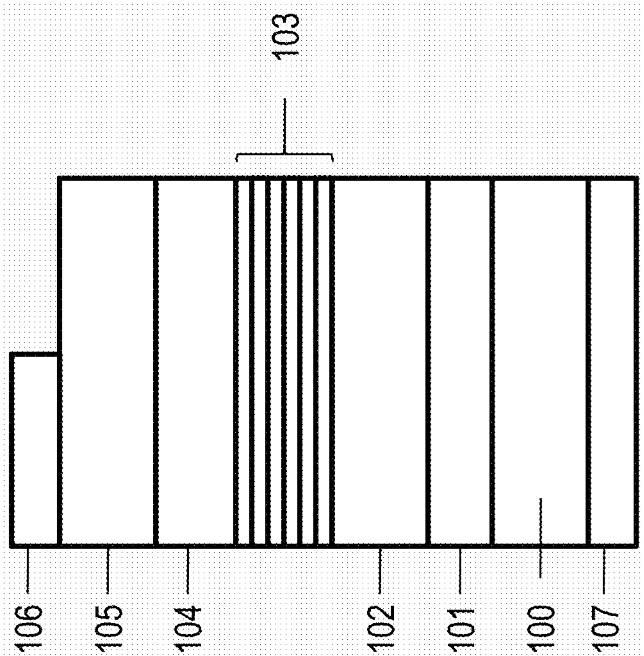
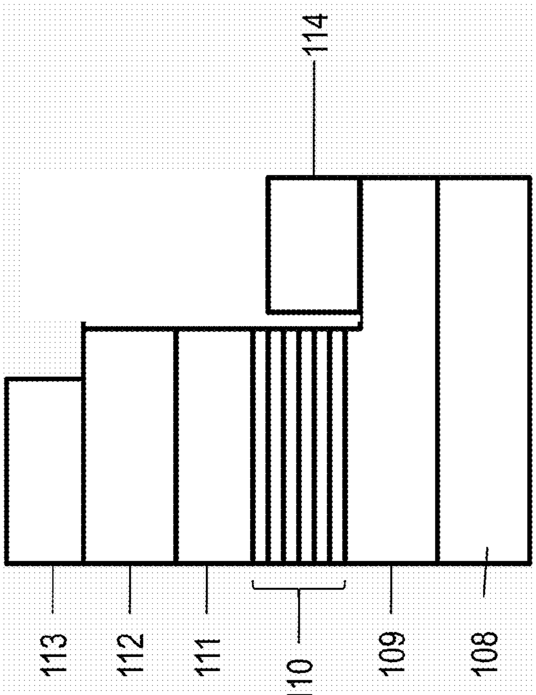
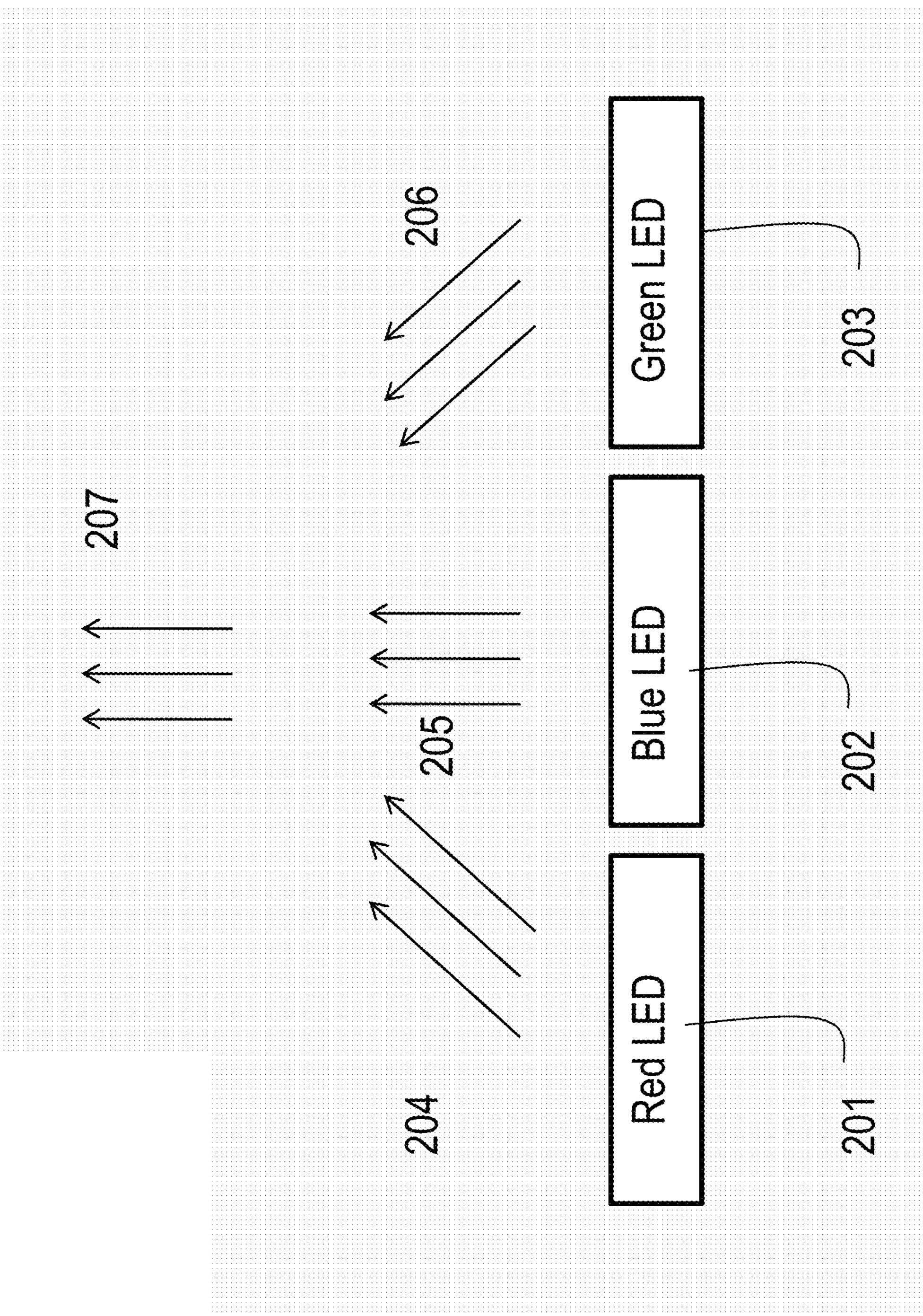


Fig. 1A (Prior art)



Green and blue LEDs. Value of x changes between green and blue colors.

Fig. 1B (Prior art)



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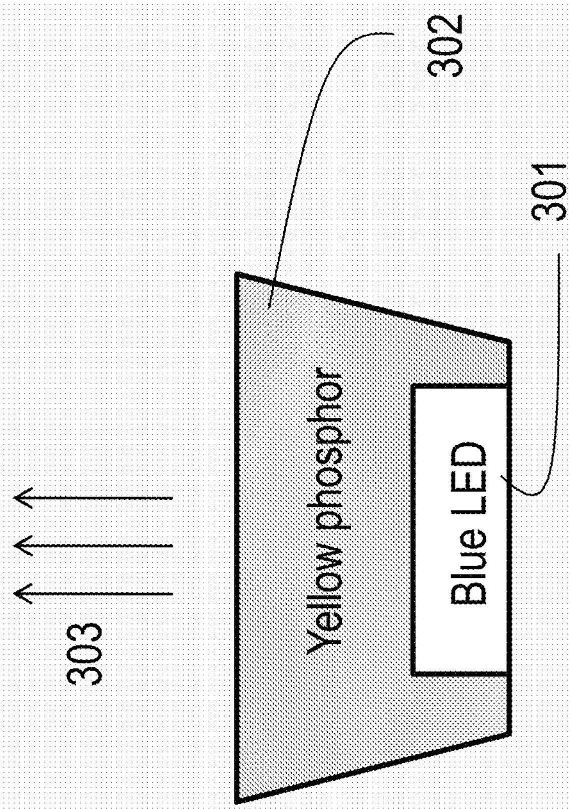

Fig. 3 (Prior art)

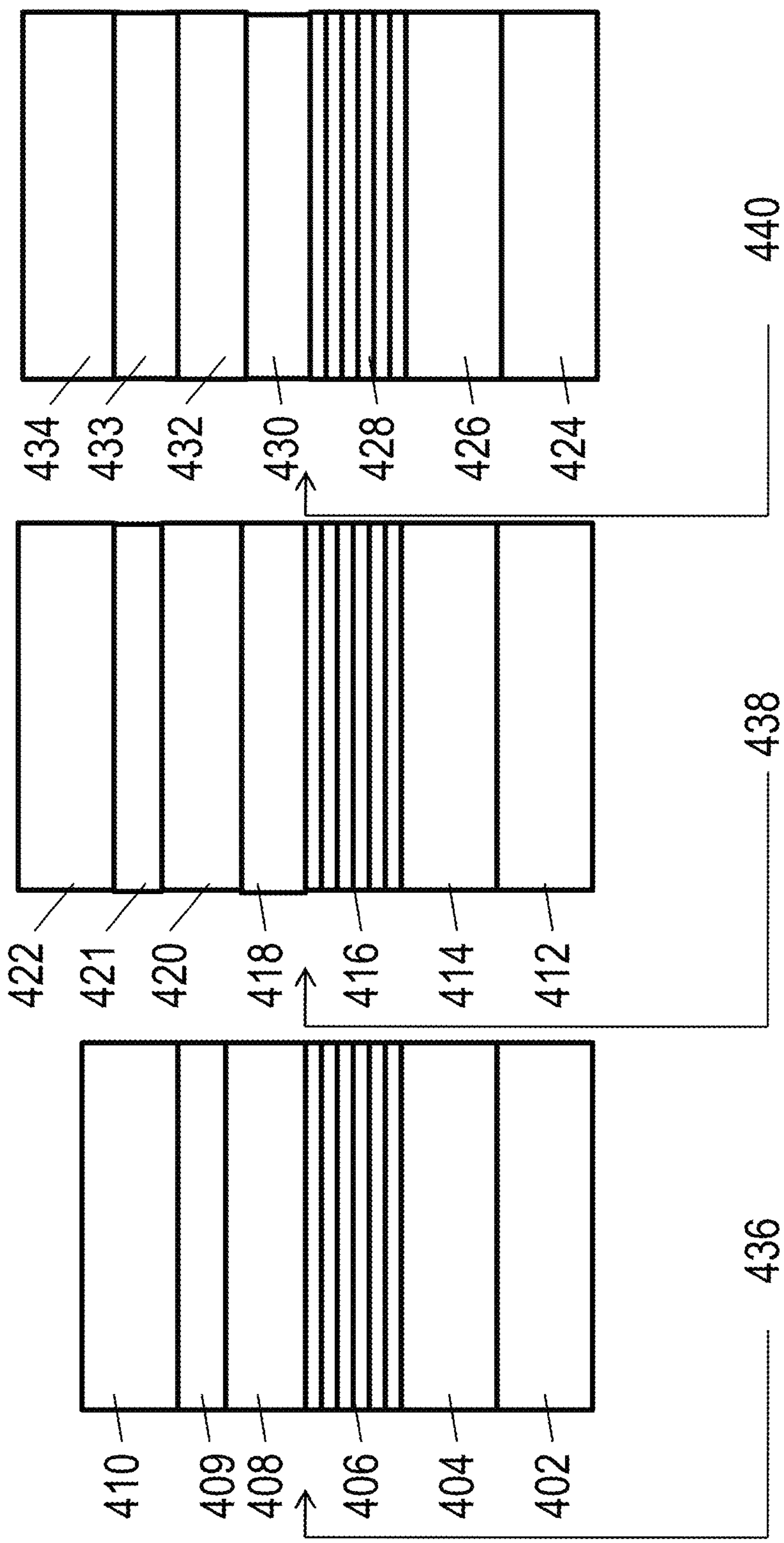

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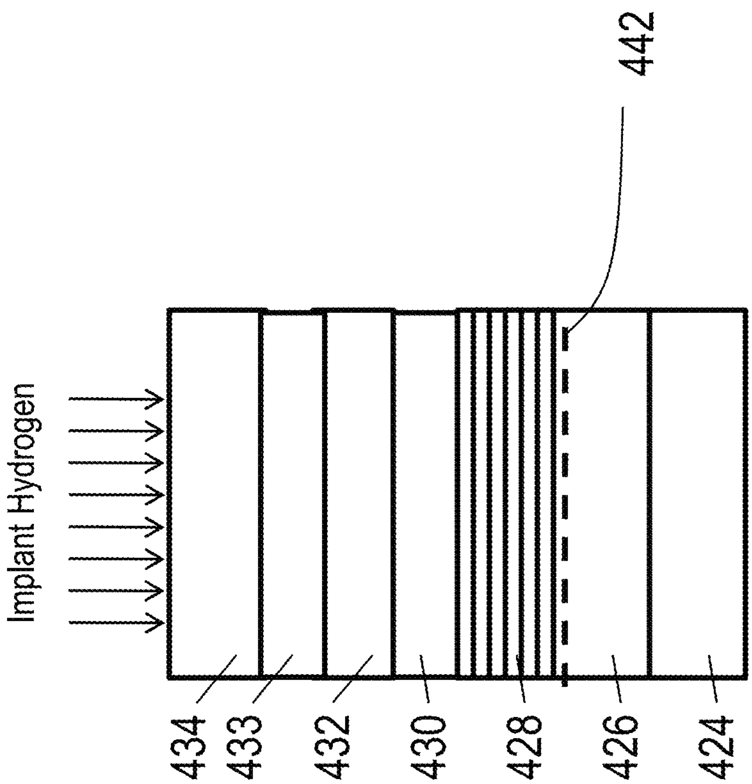
Fig. 4A



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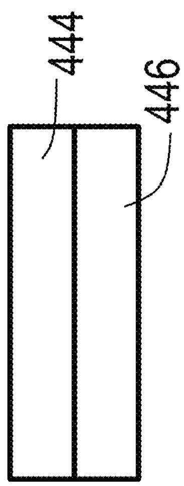

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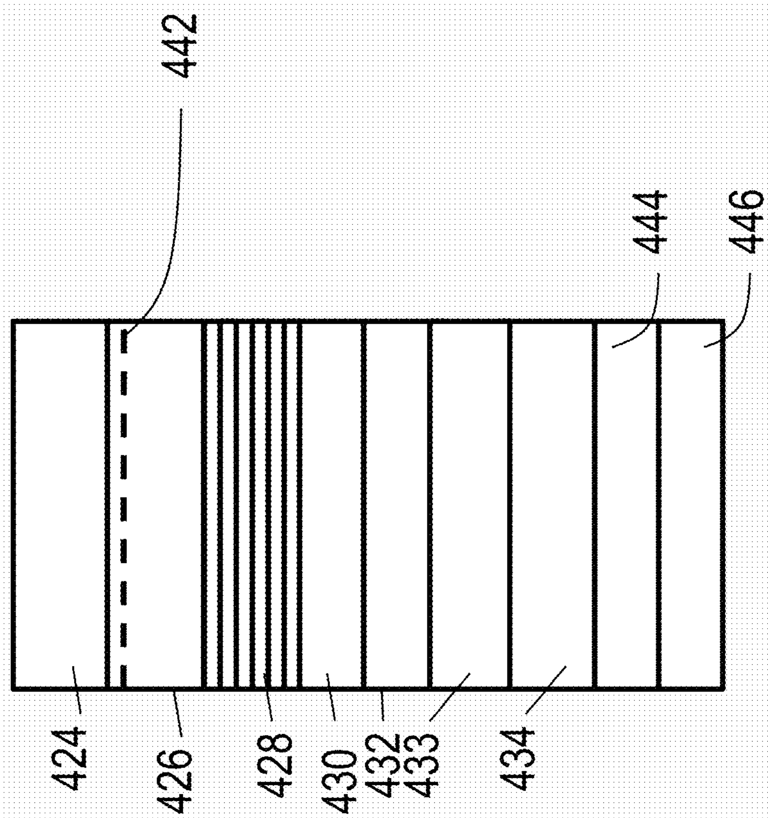

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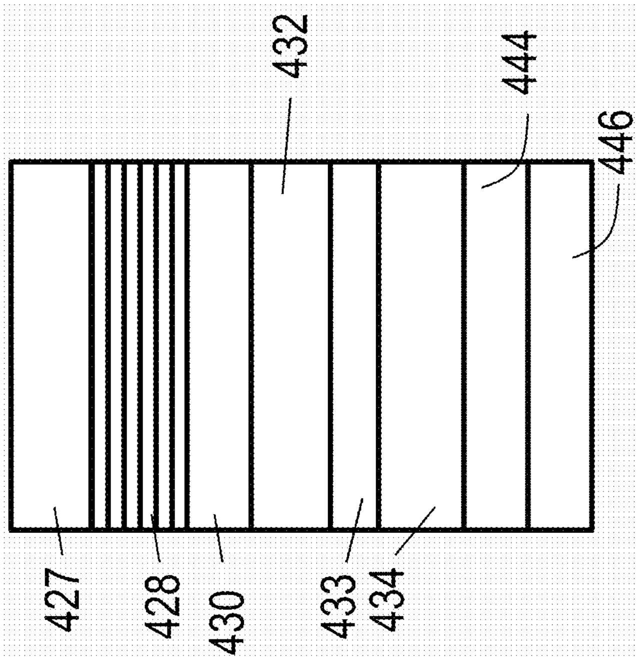

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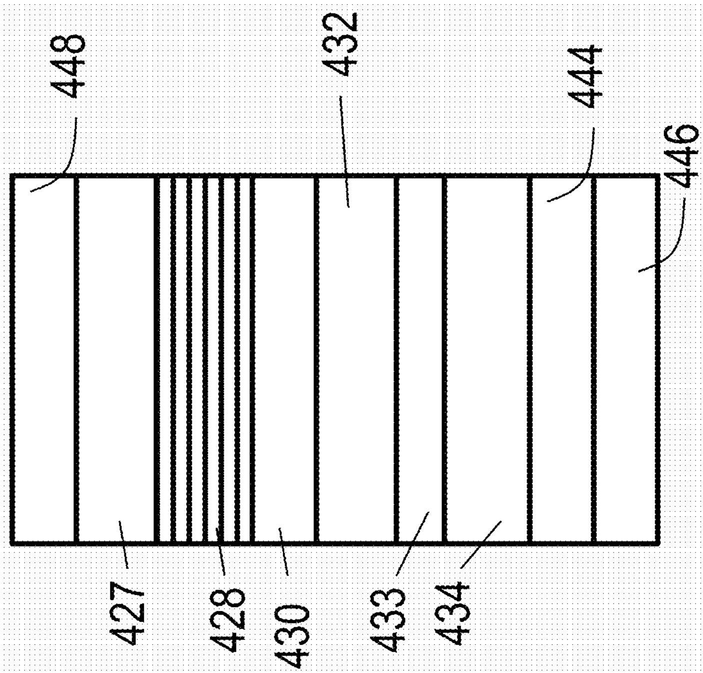

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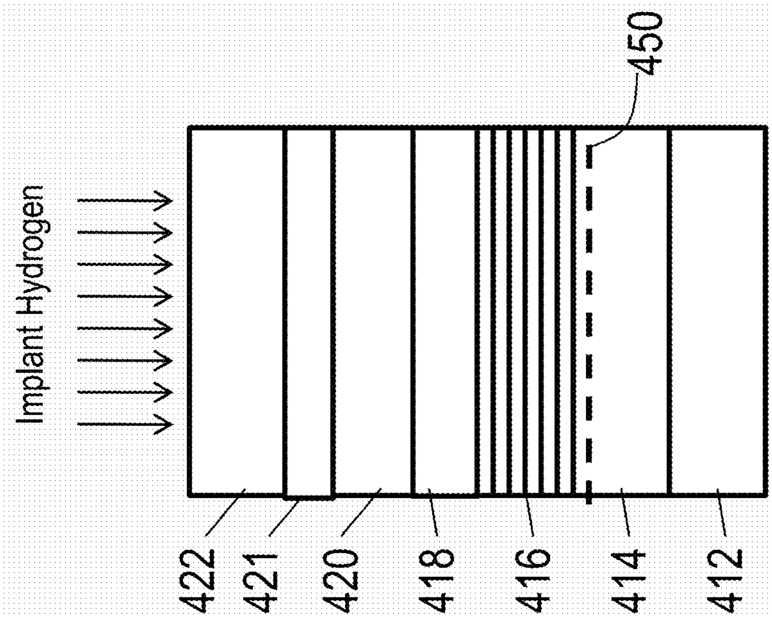

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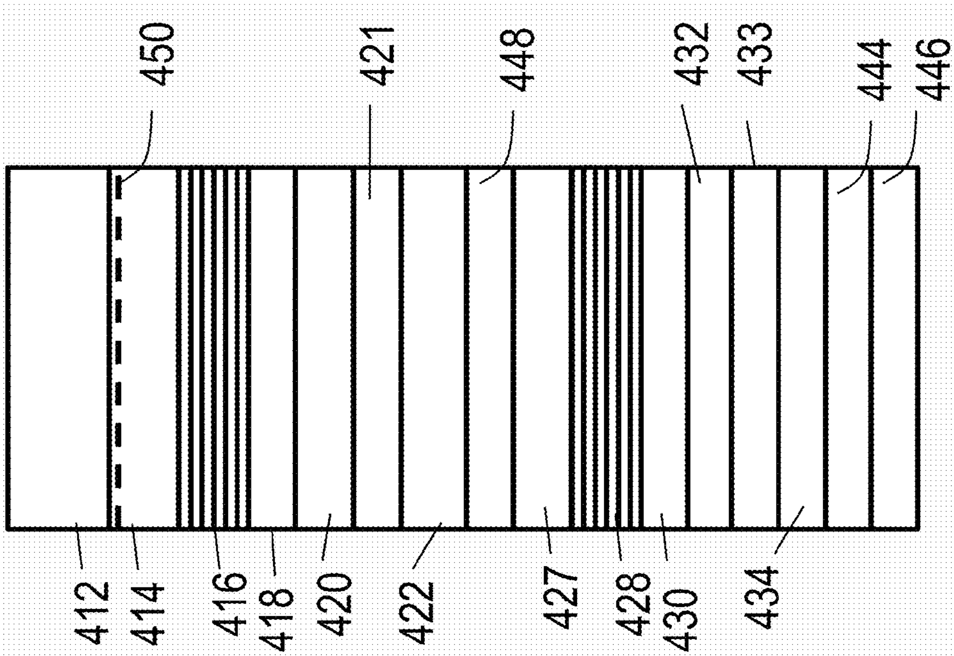
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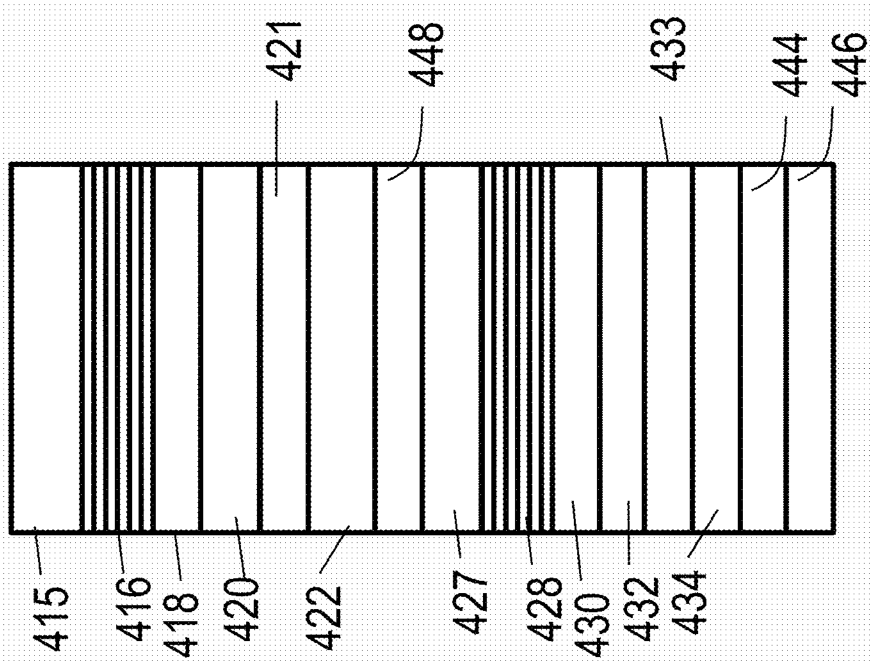
Fig. 4H



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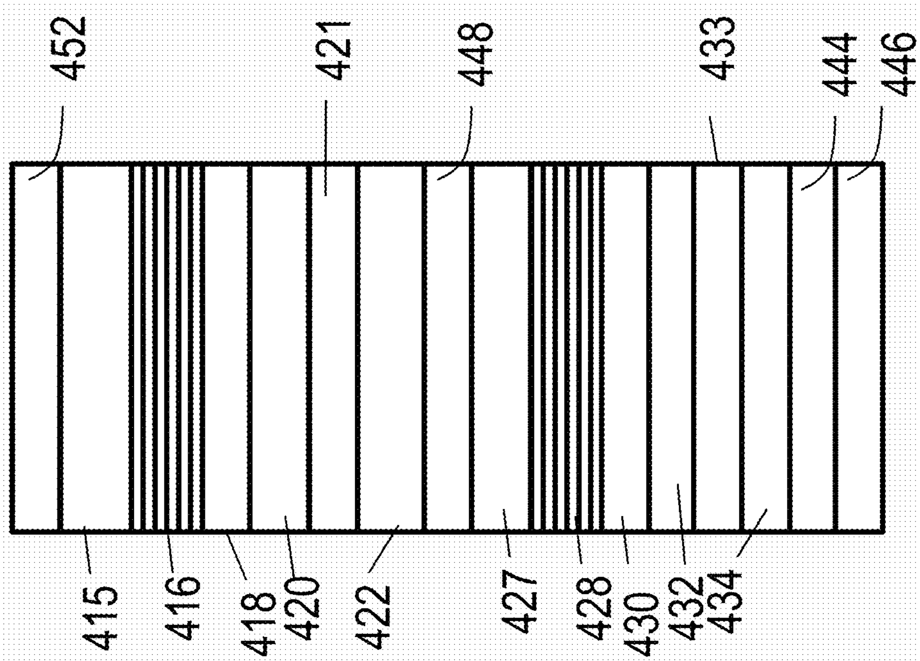

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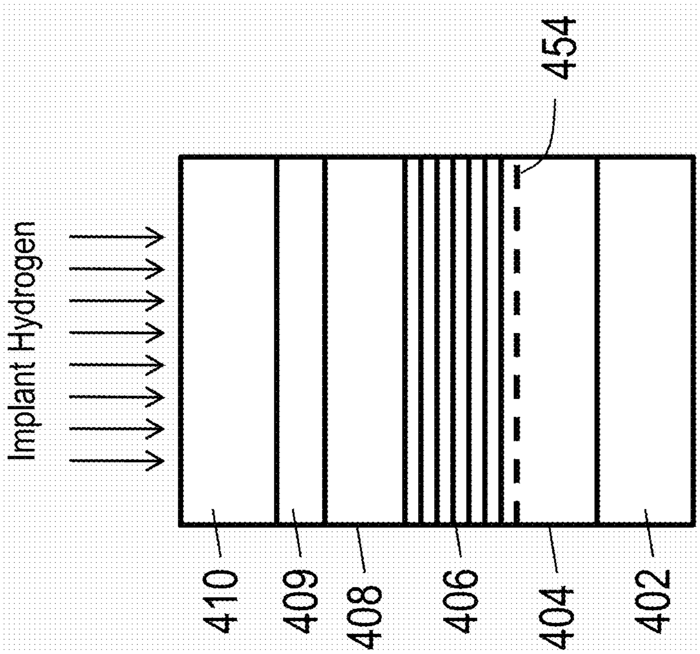

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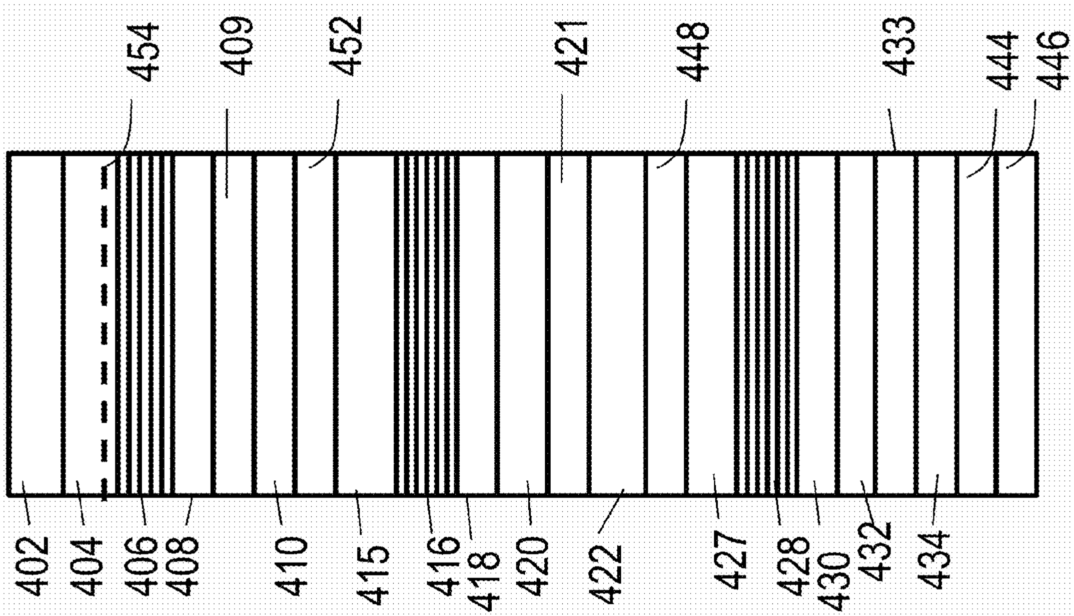

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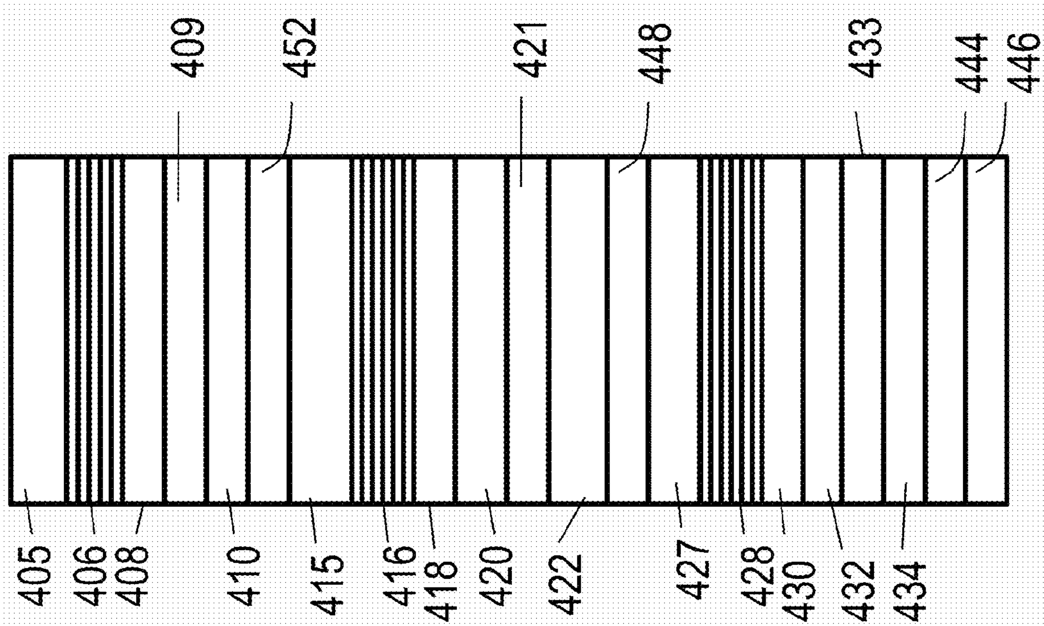
Fig. 4L

Fig. 4M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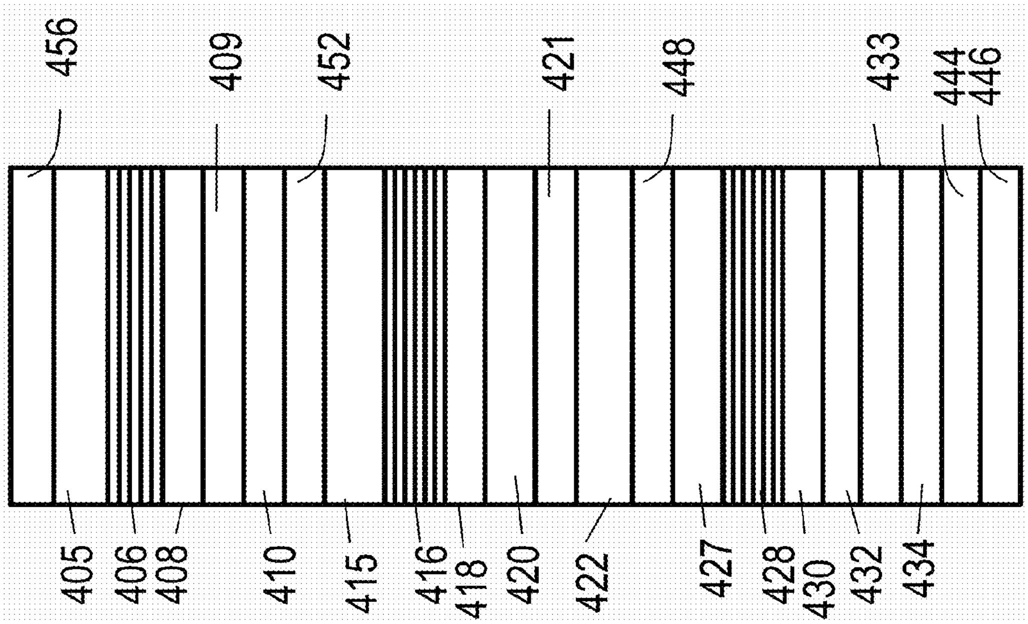
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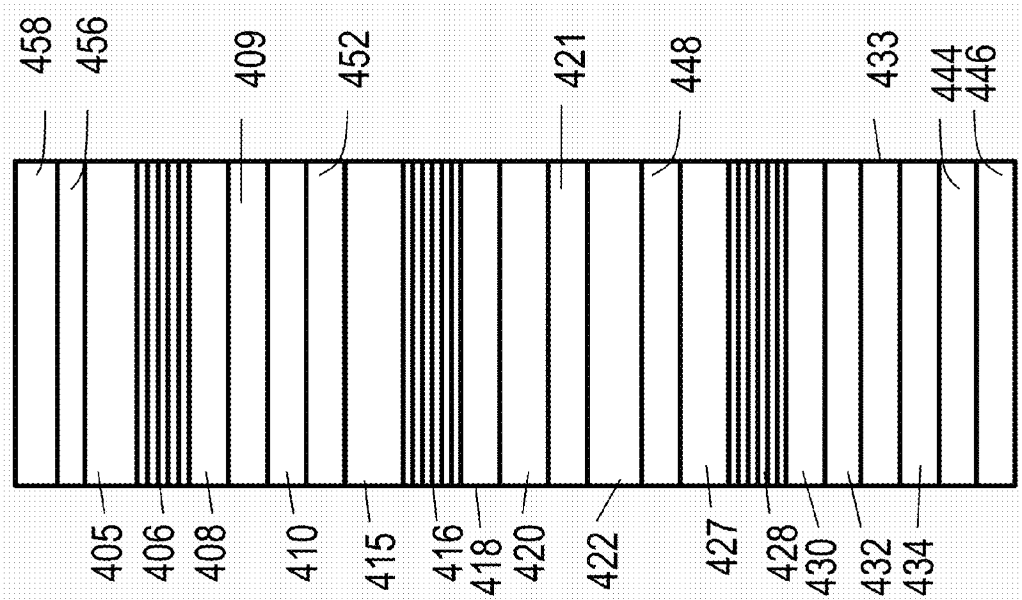
Fig. 4N

Fig. 4O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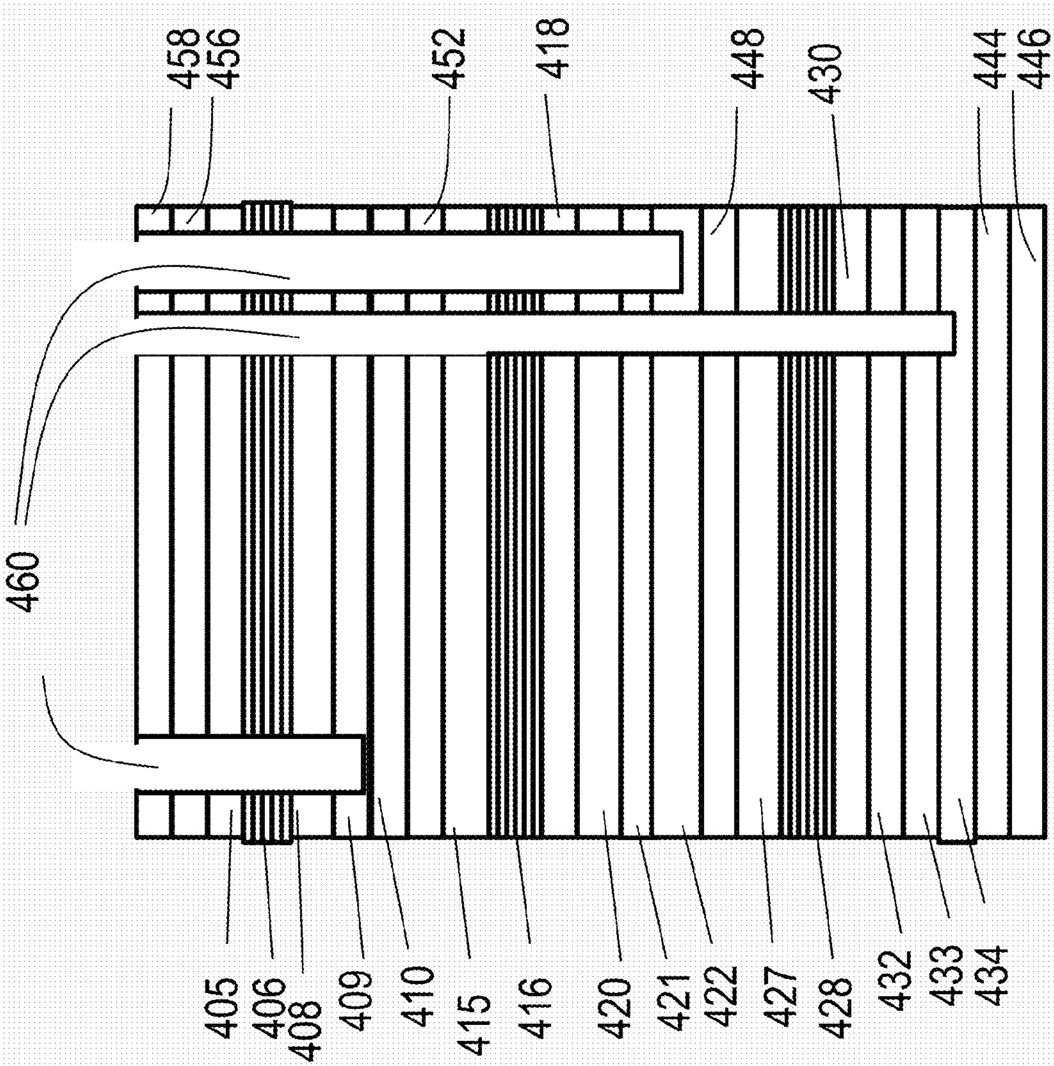
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Fig. 4P

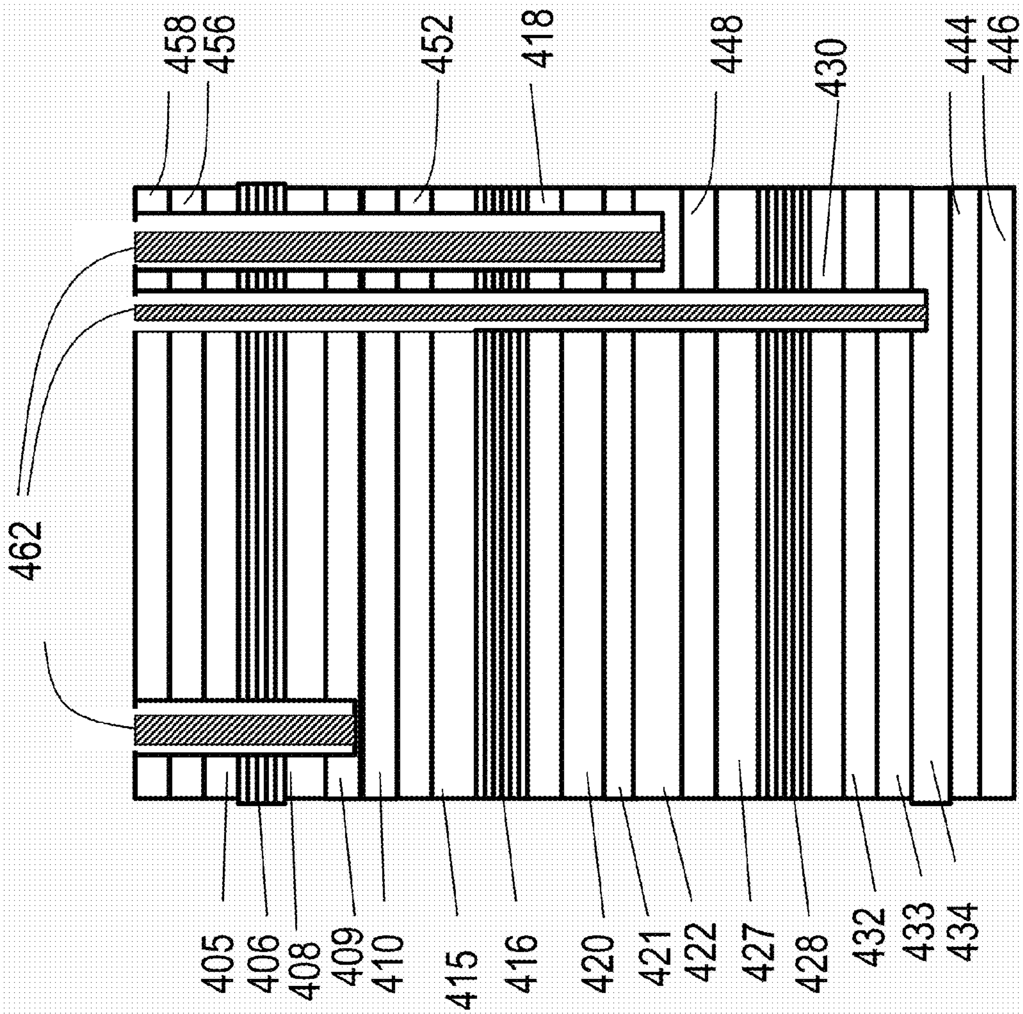
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Fig. 4Q

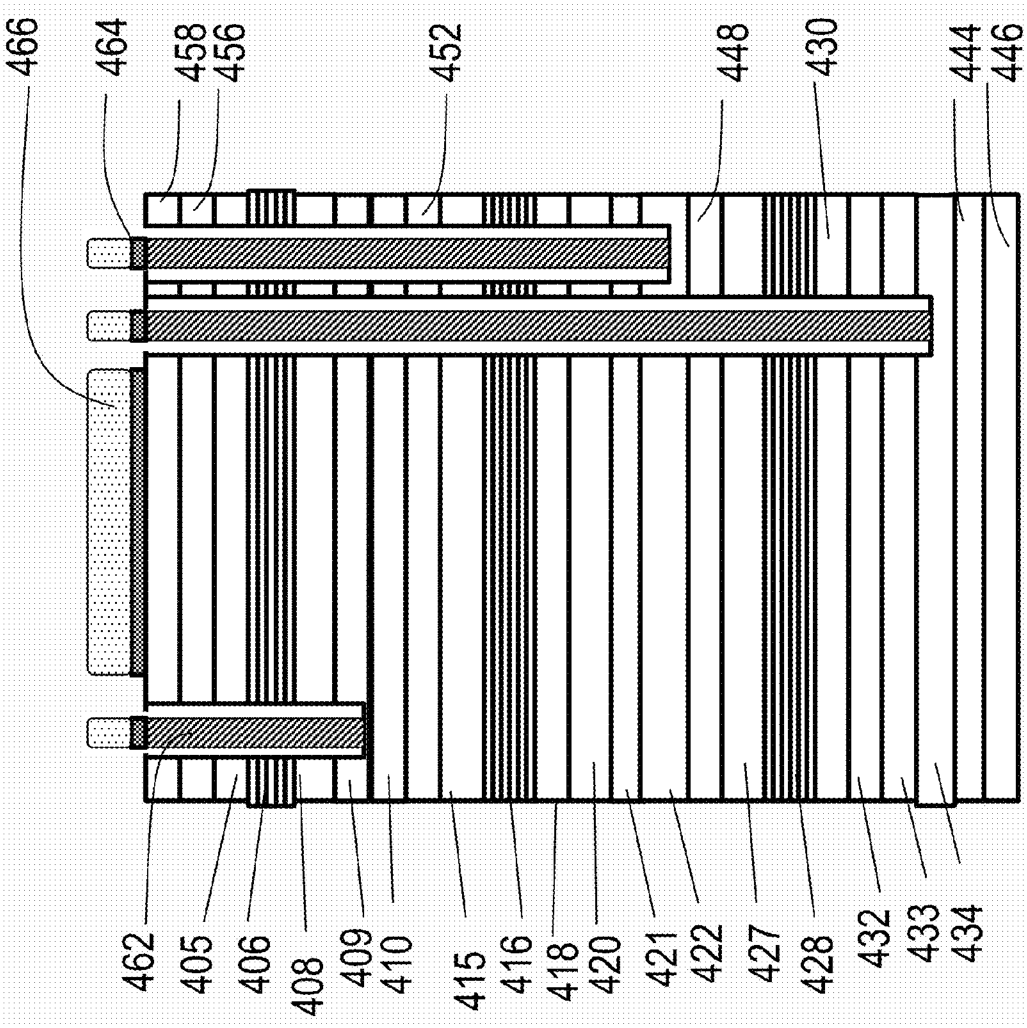
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Fig. 4R

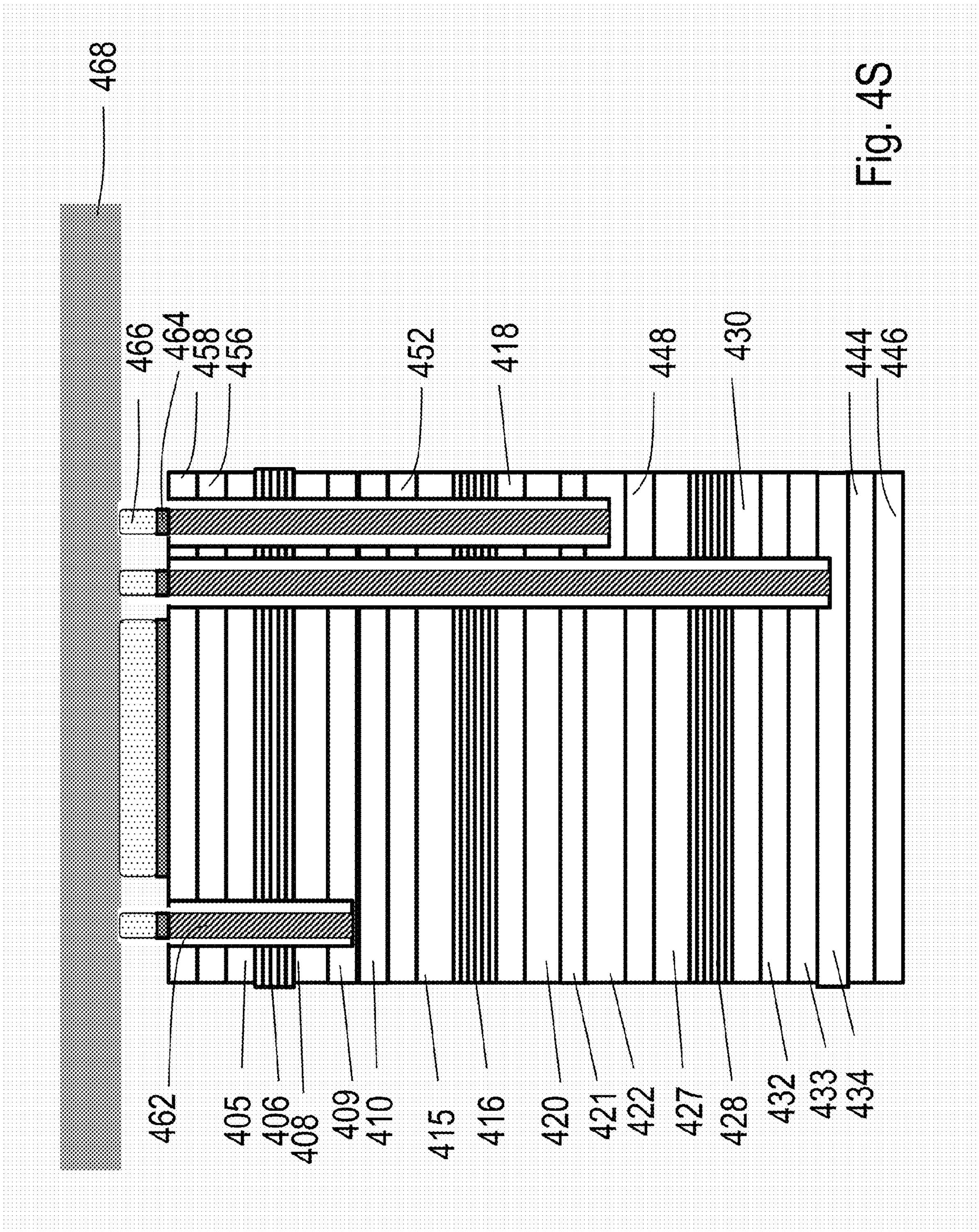
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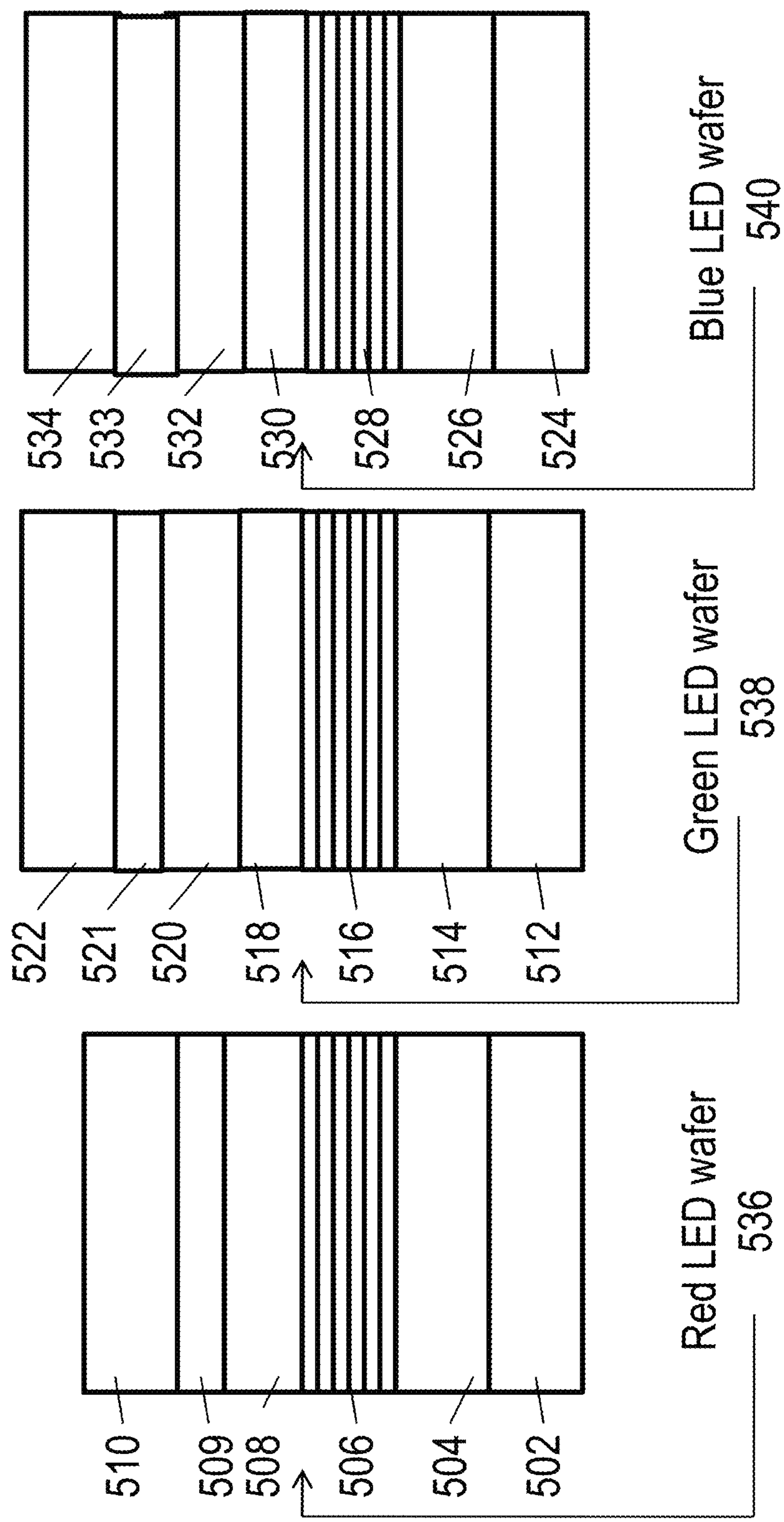
Fig. 4S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Blue LED wafer
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Fig. 5A

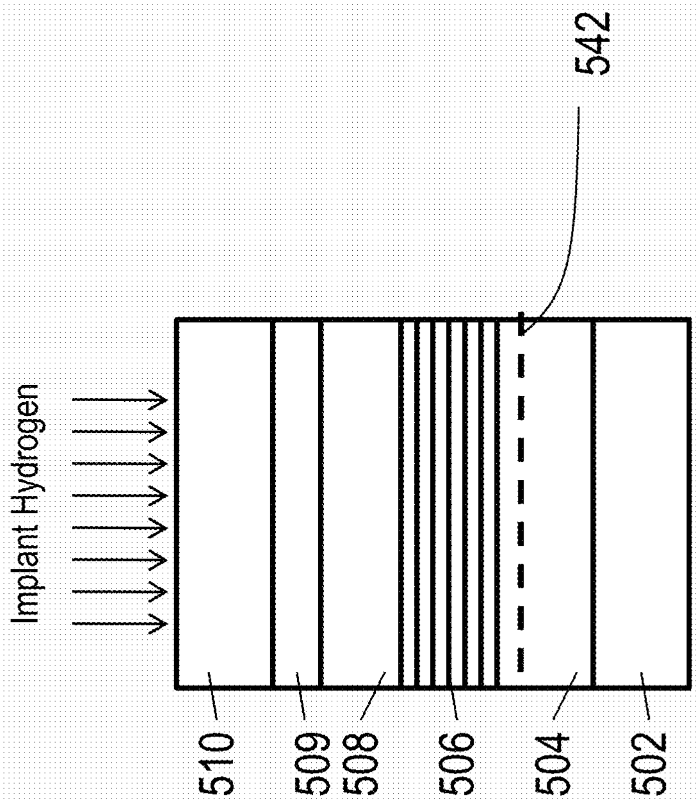
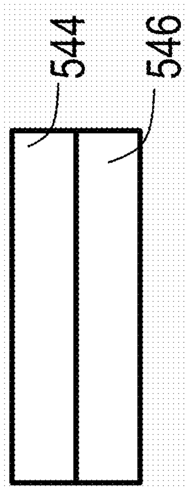


Fig. 5B



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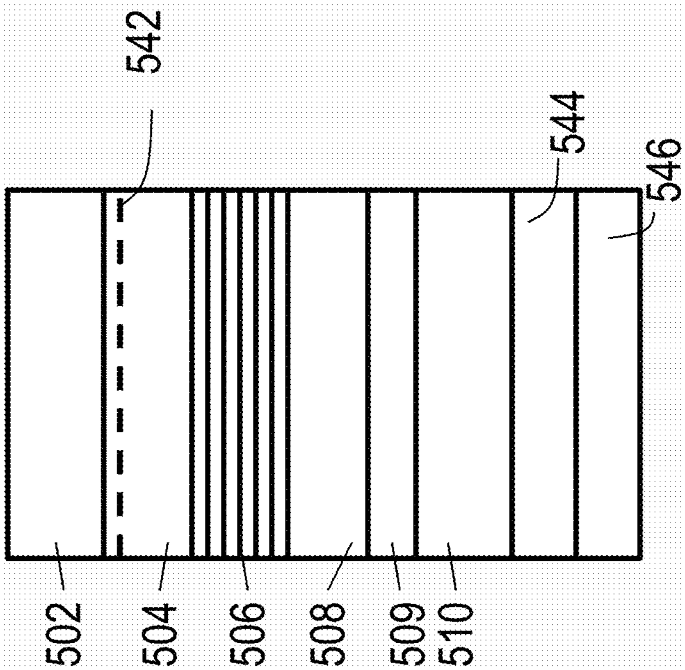

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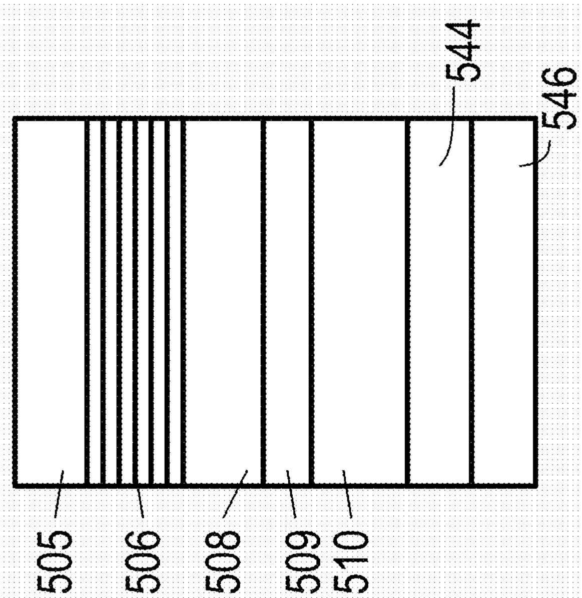

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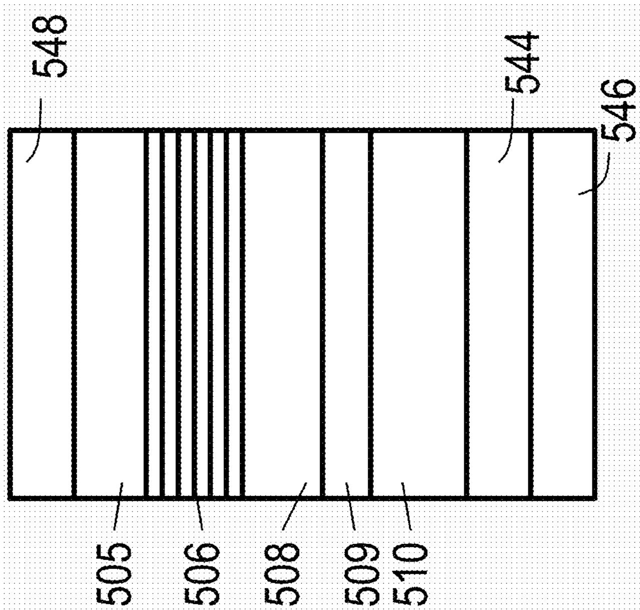

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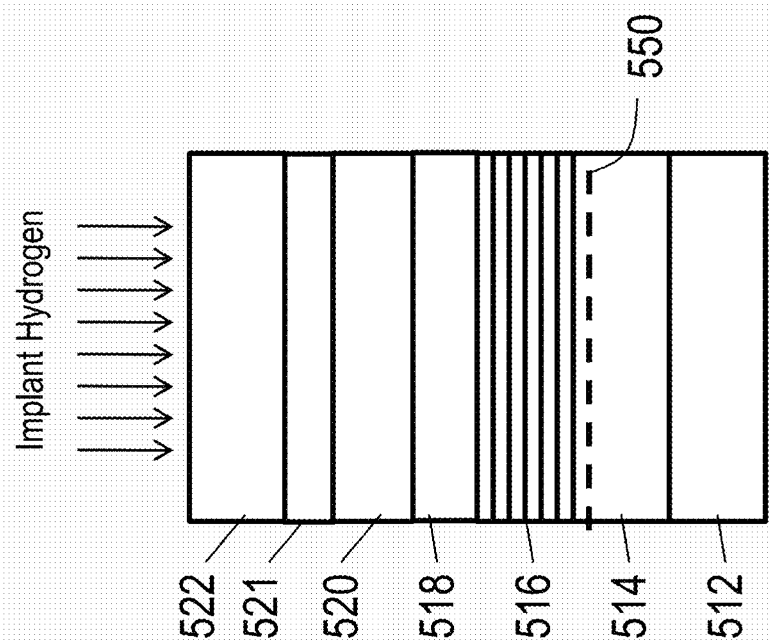

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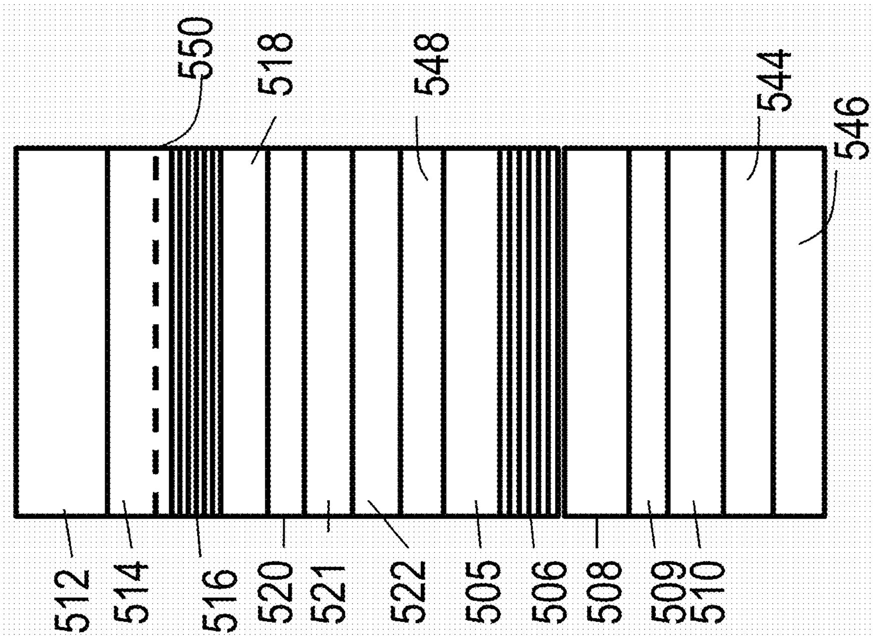

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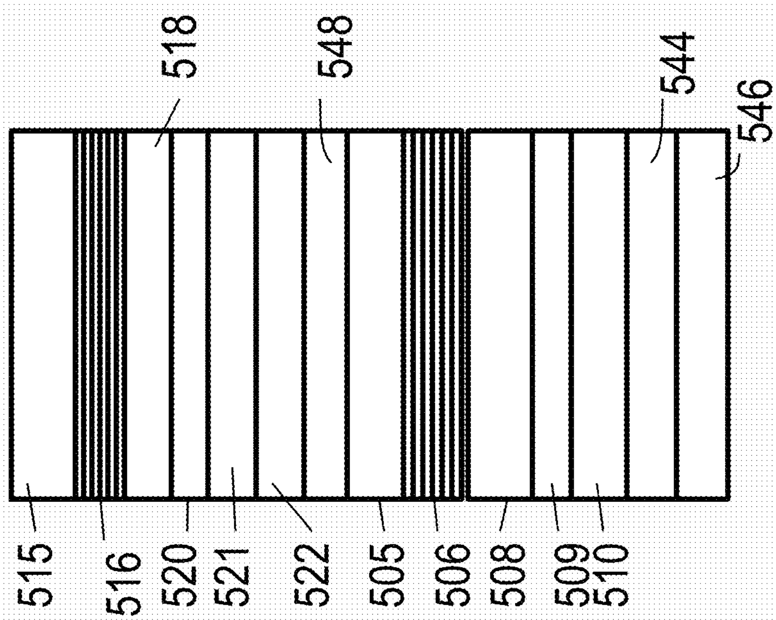

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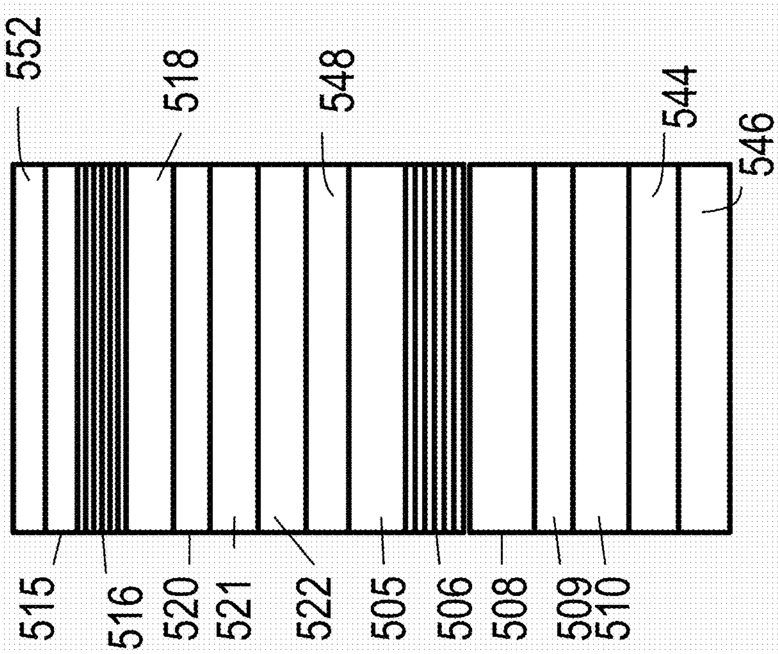

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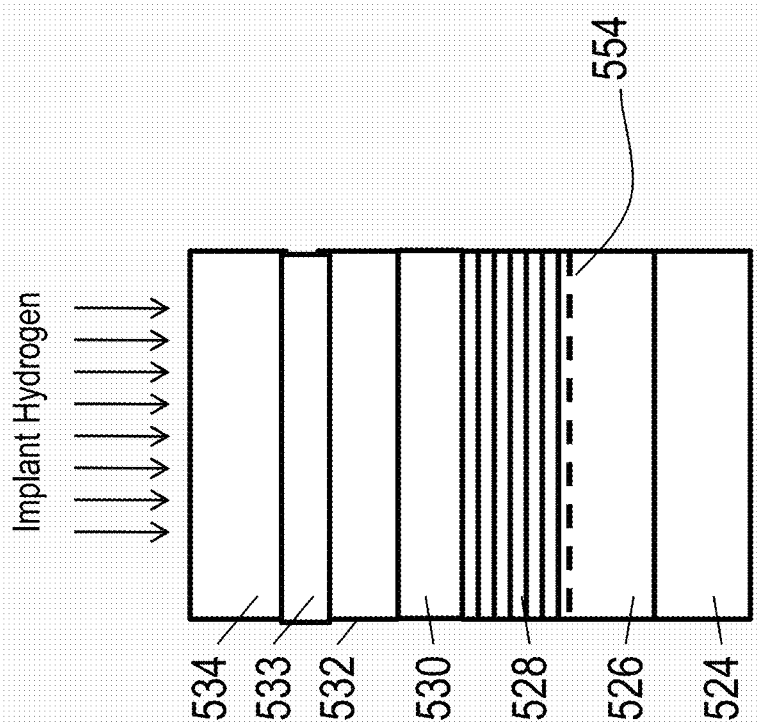

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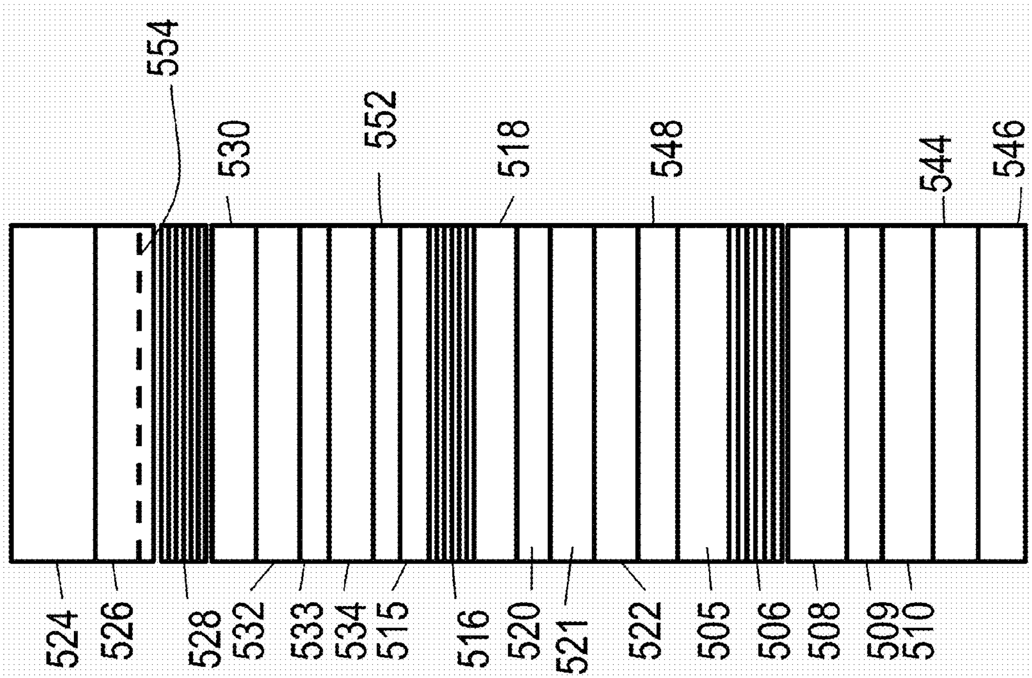
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Fig. 5L

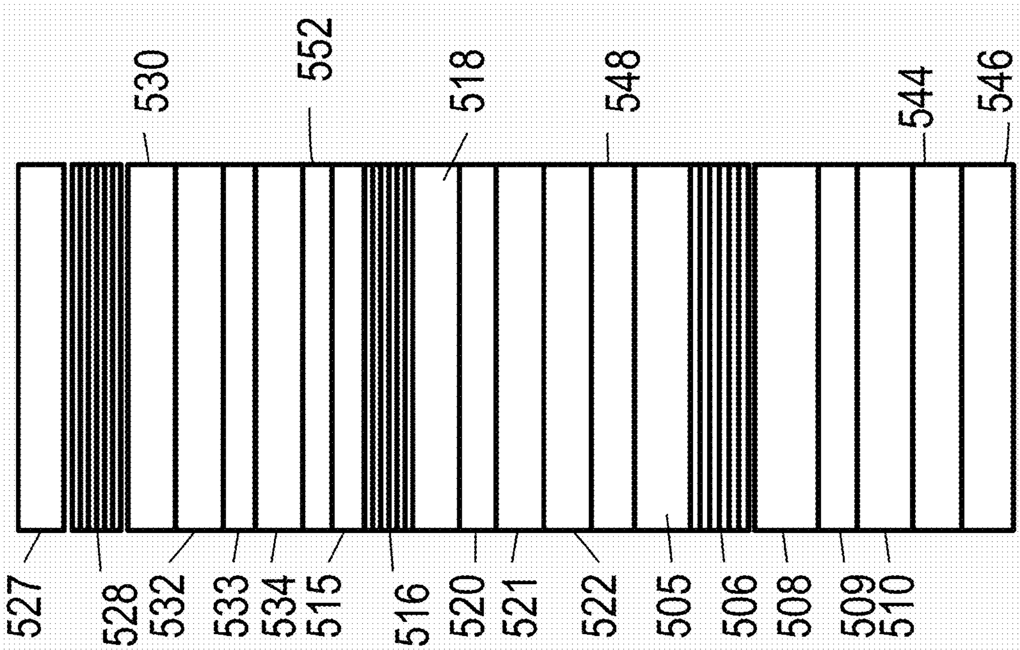
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Fig. 5M

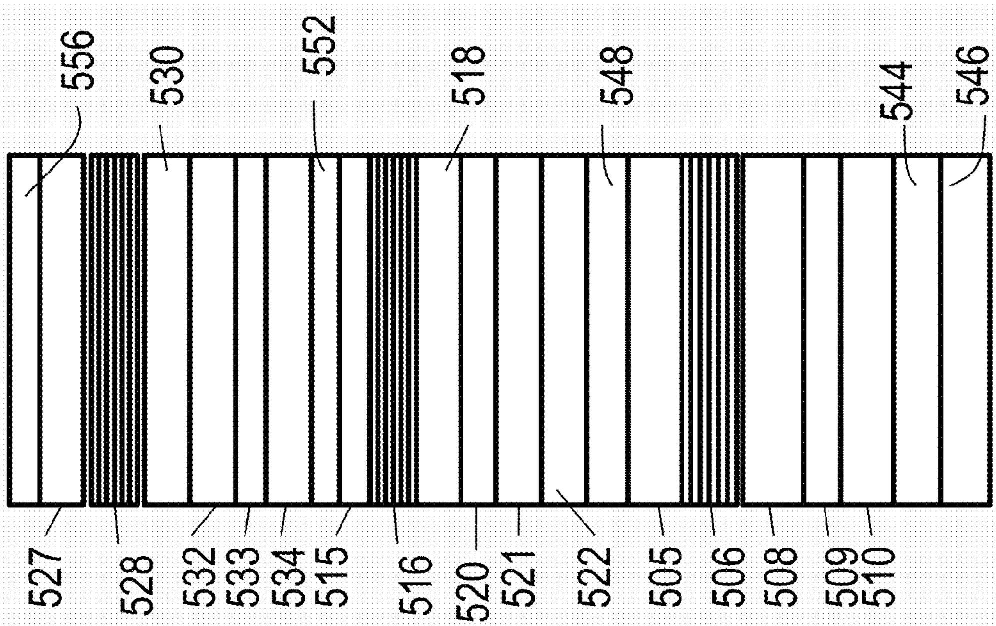
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Fig. 5N

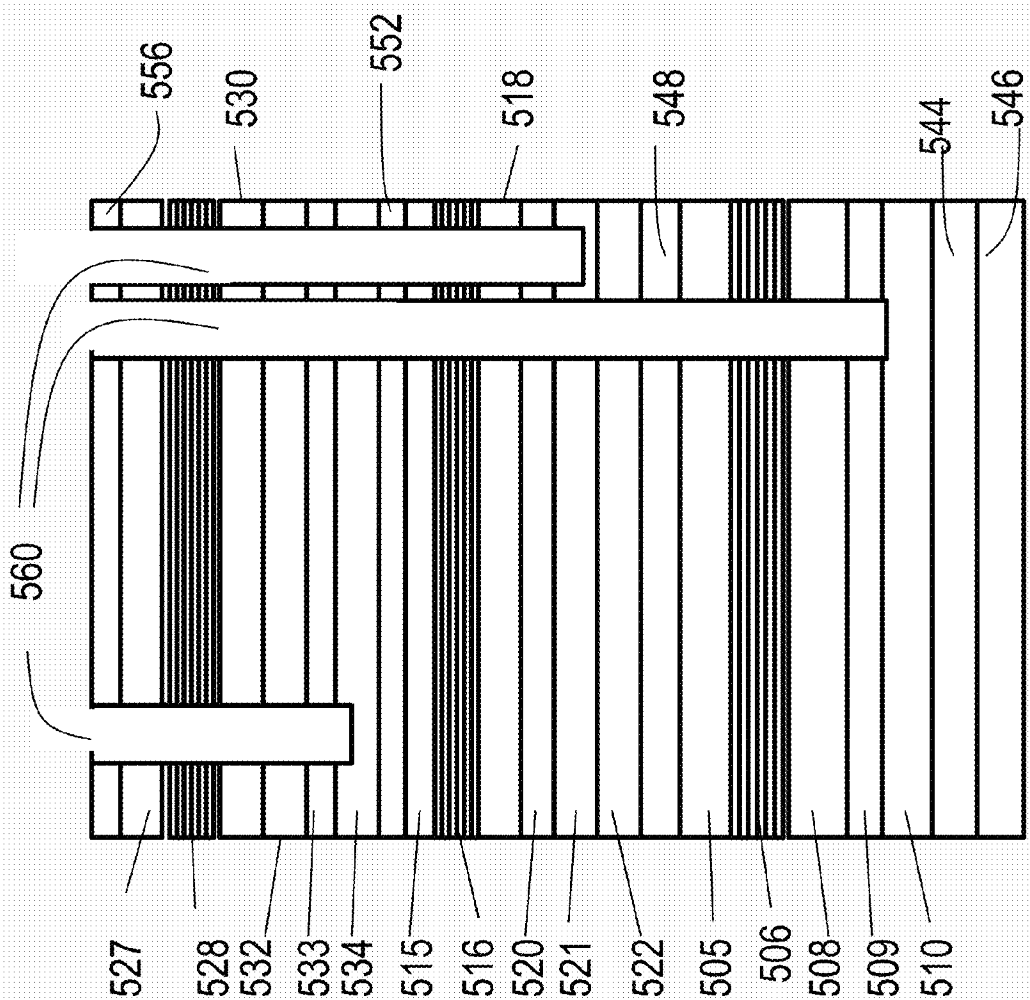
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Fig. 5O

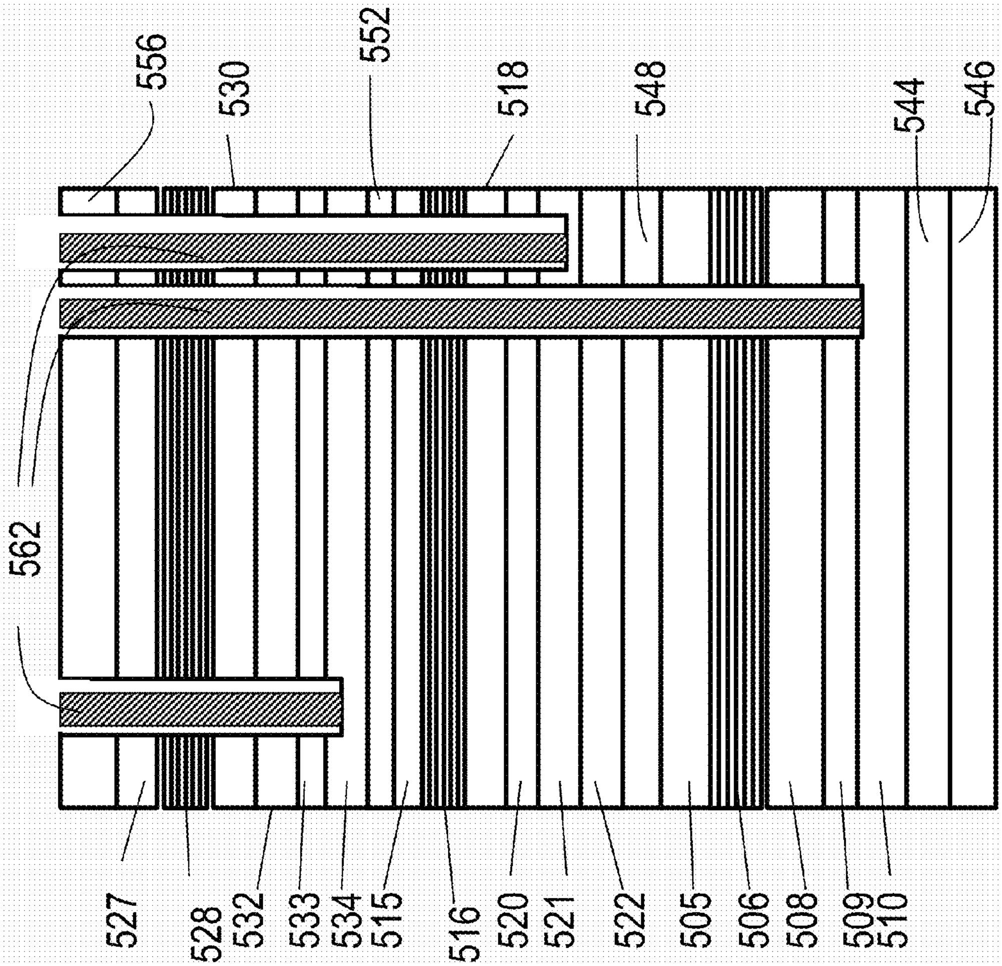
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Fig. 5P

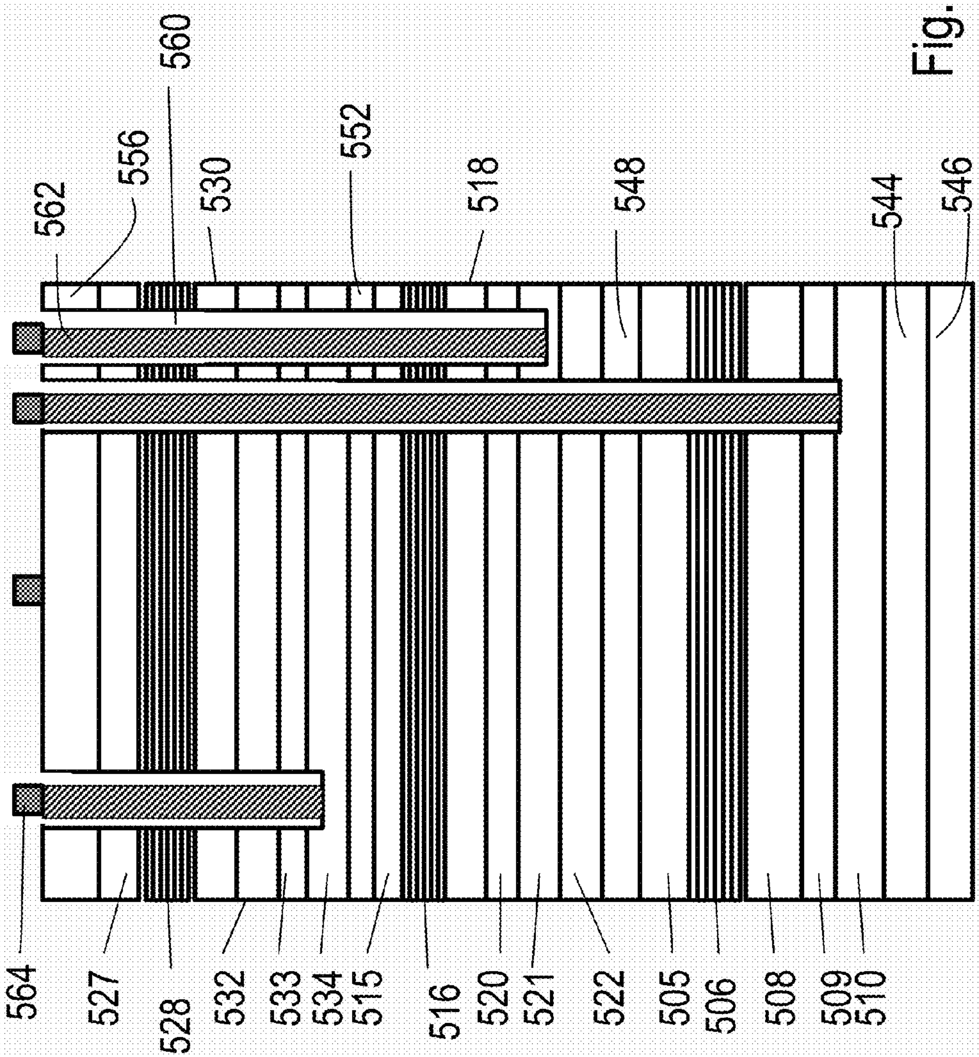
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Fig. 5Q

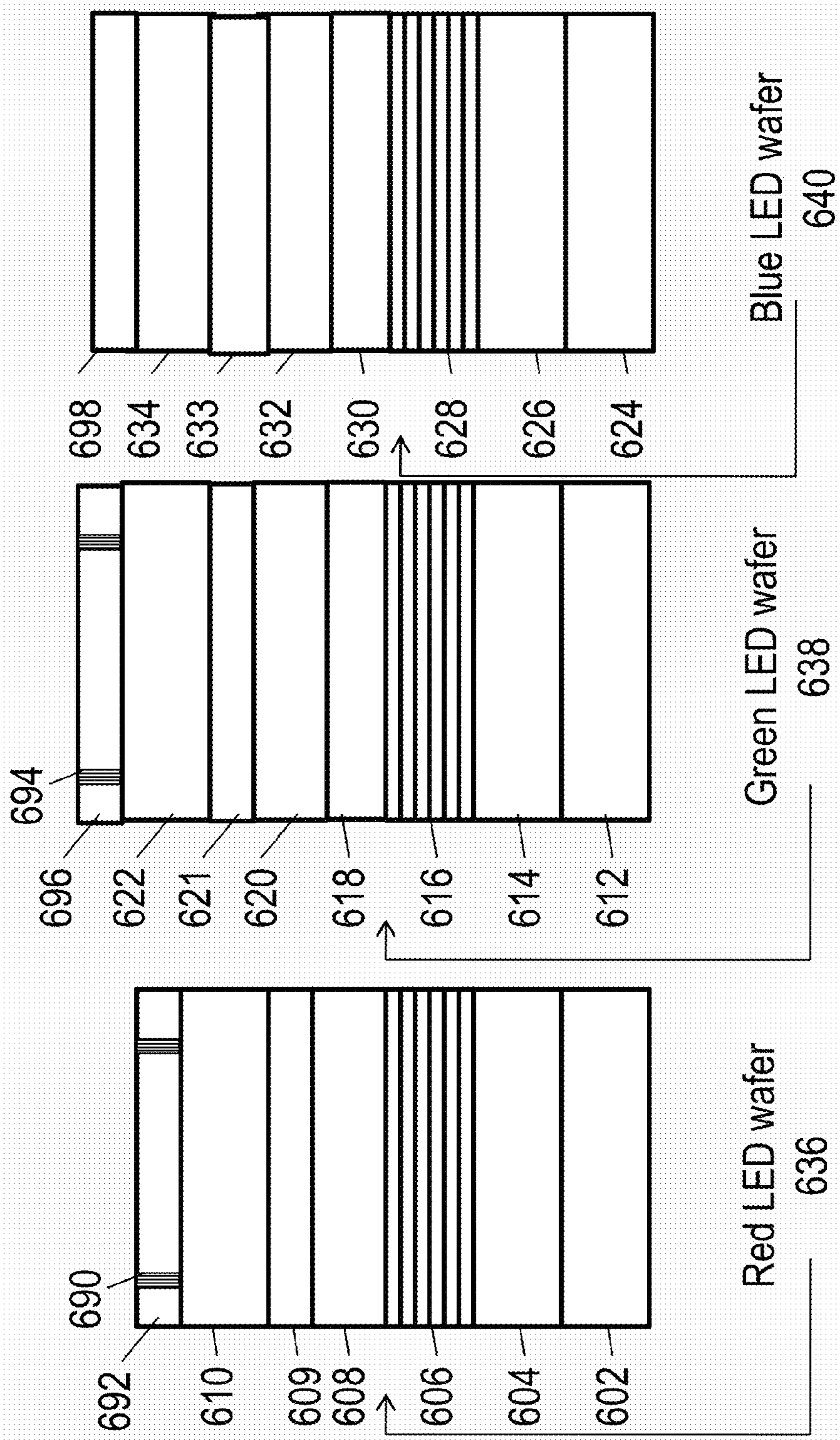

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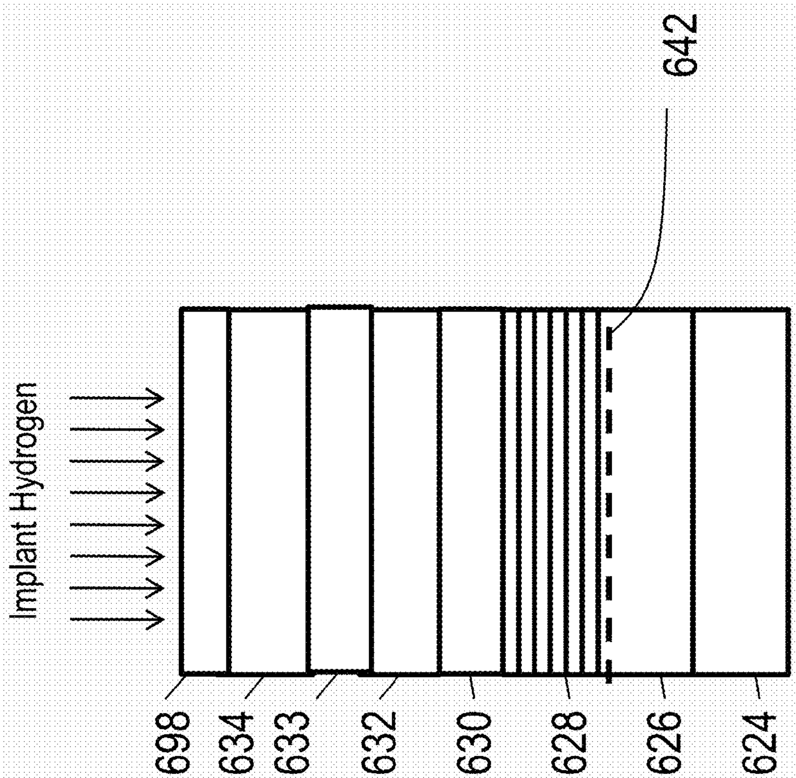
Fig. 6A



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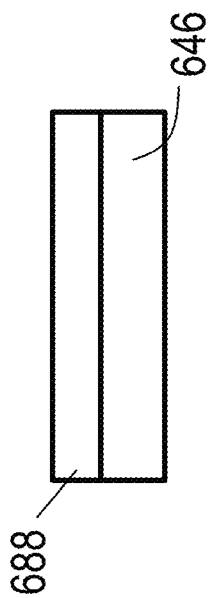


Fig. 6C

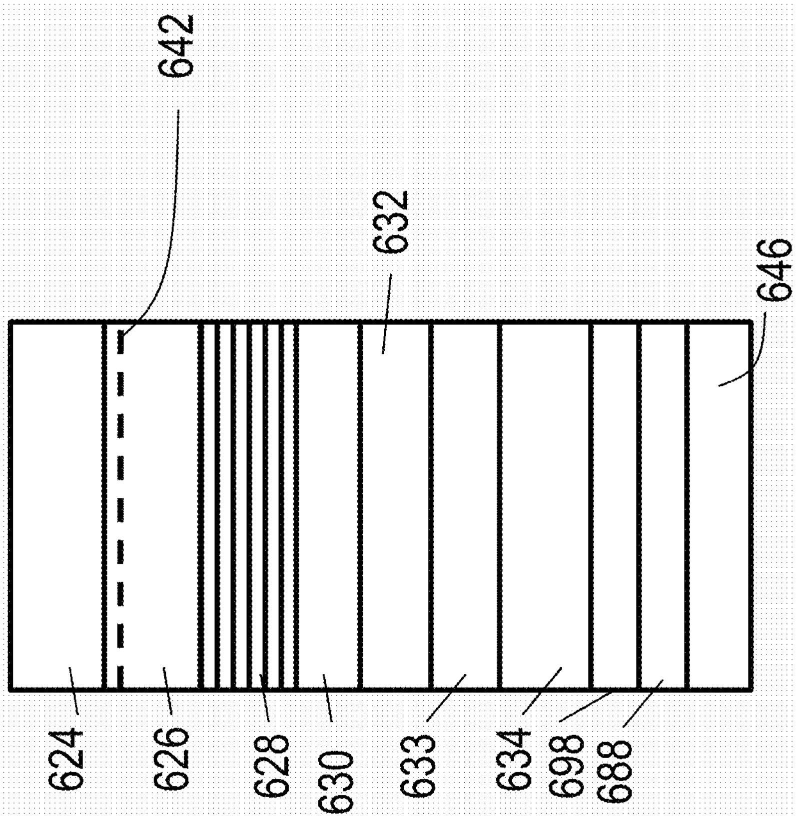


Fig. 6D

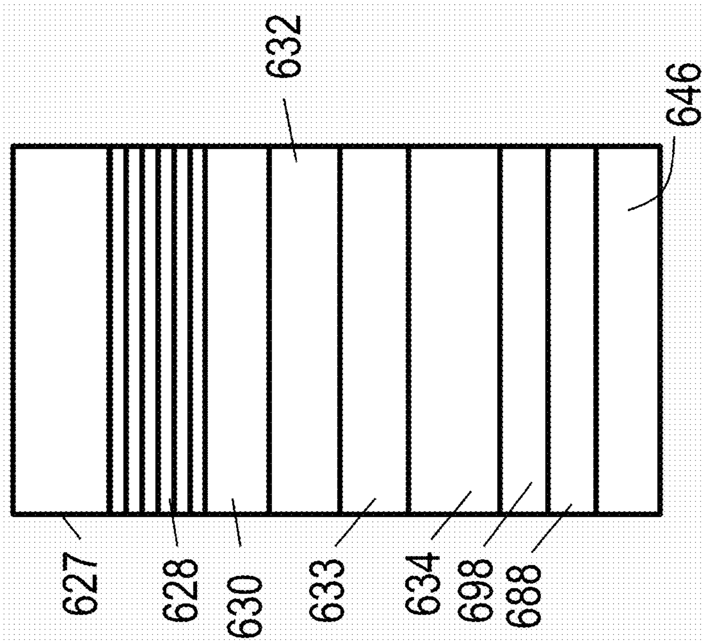


Fig. 6E

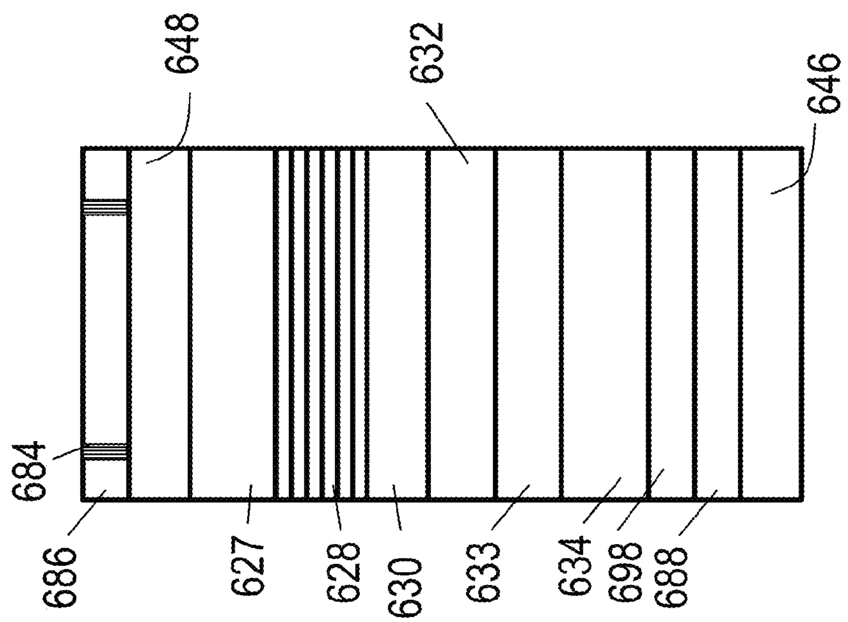


Fig. 6F

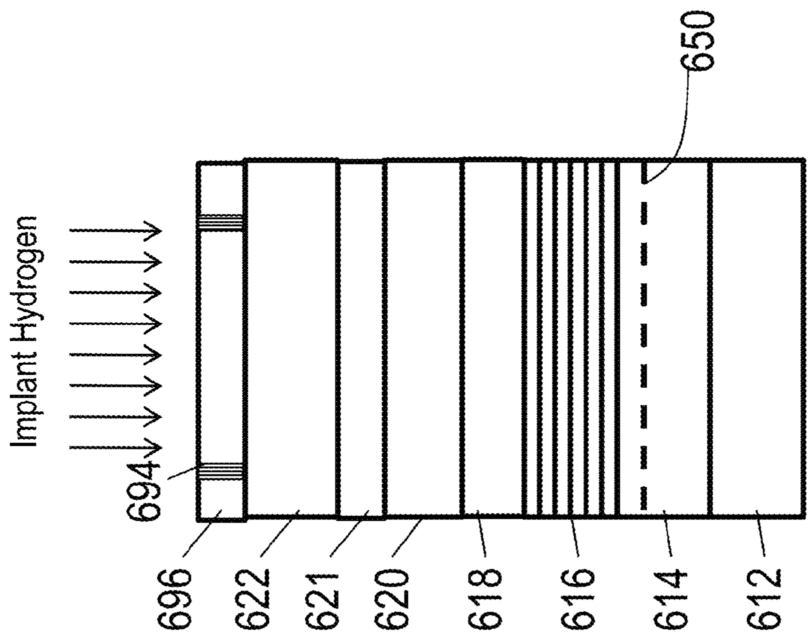


Fig. 6G

Fig. 6H

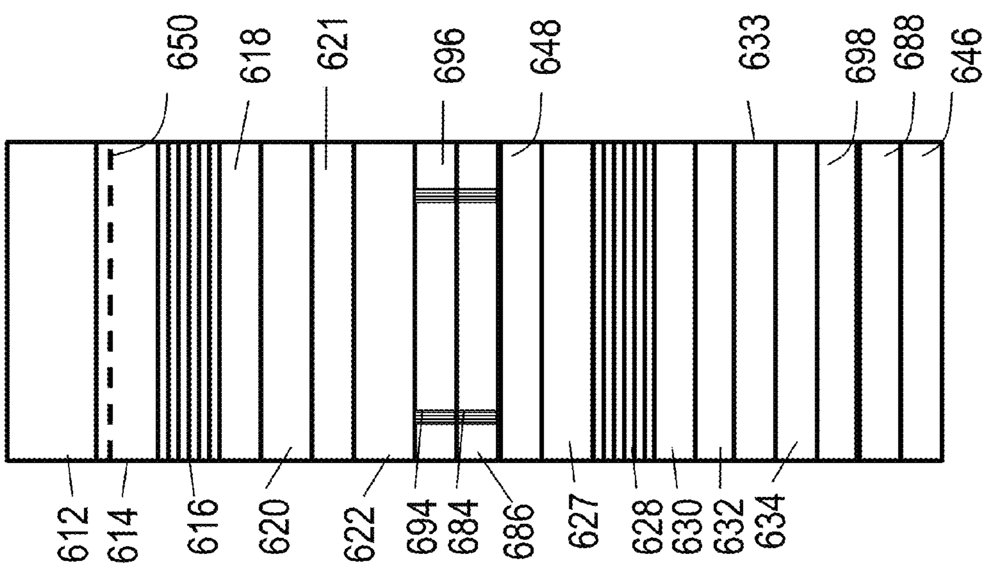

650
618
621
696
648
633
698
688
646
612
614
616
620
622
694
684
686
627
628
630
632
634

Fig. 6I

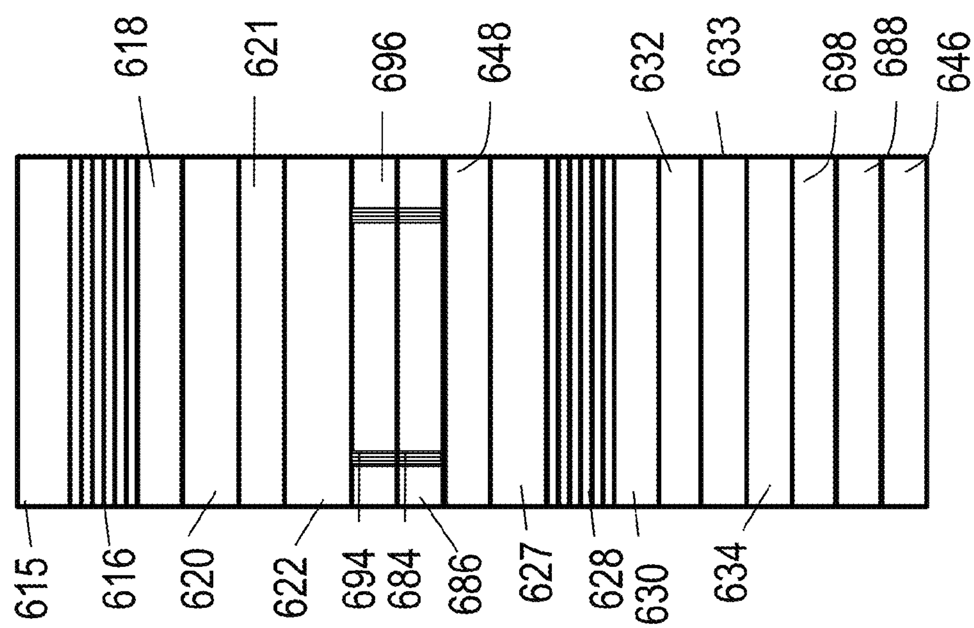

618
621
696
648
632
633
698
688
646
615
616
620
622
694
684
686
627
628
630
634

Fig. 6J

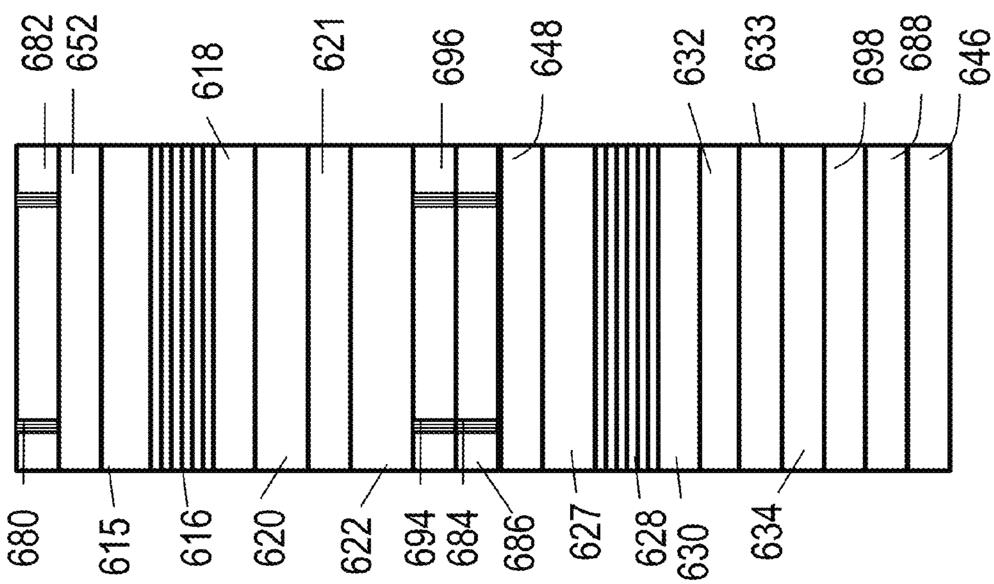
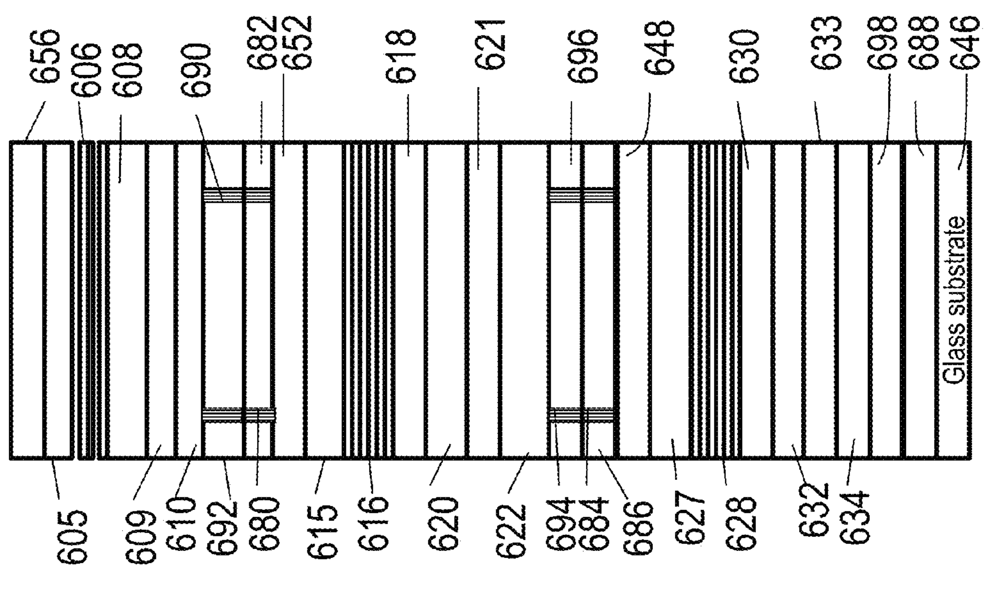

682
652
618
621
696
648
632
633
698
688
646
680
615
616
620
622
694
684
686
627
628
630
634

Fig. 6K


656
606
608
690
682
652
618
621
696
648
630
633
698
688
646
Glass substrate
605
609
610
692
680
615
616
620
622
694
684
686
627
628
632
634

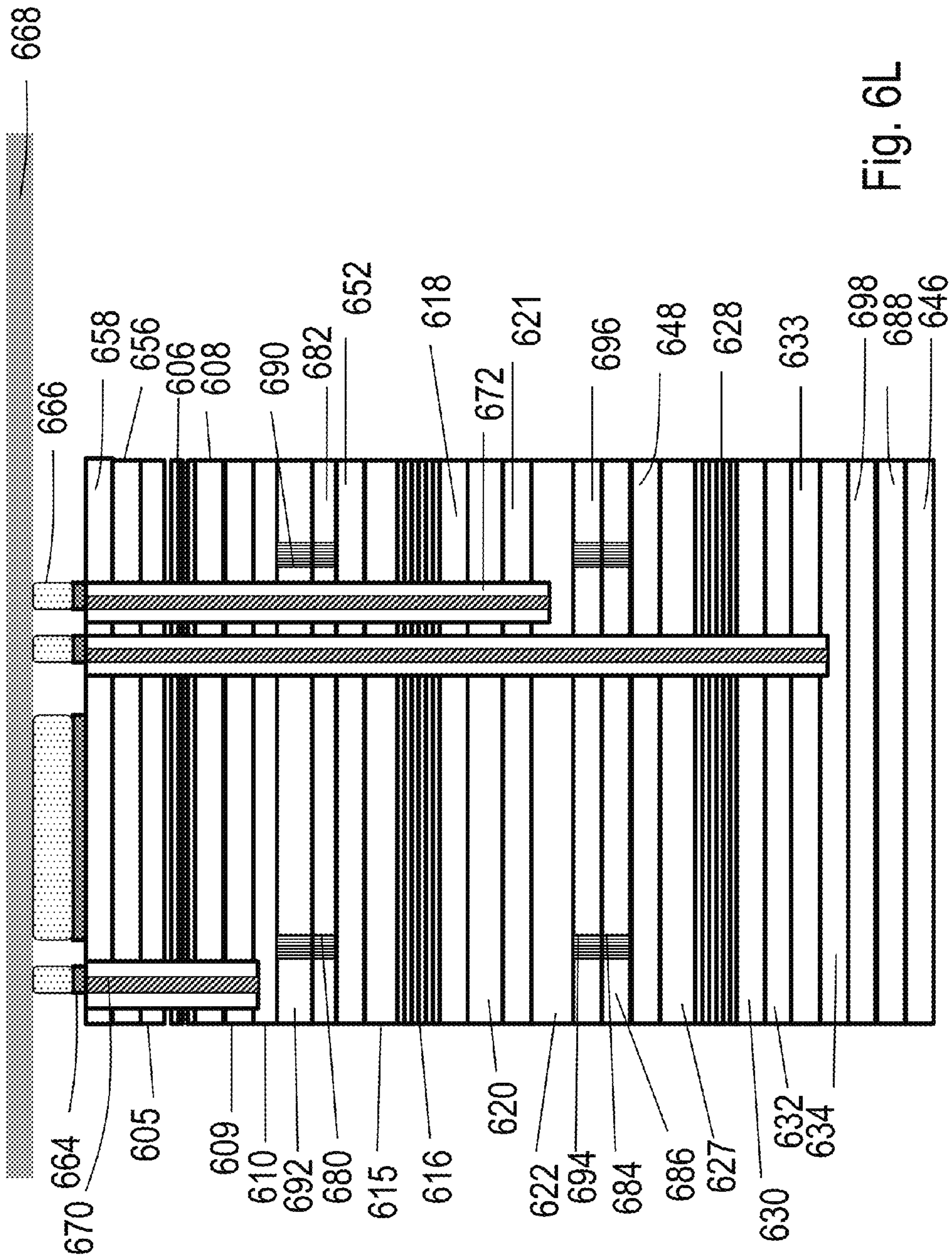

668
666
658
656
606
608
690
682
652
618
672
621
696
648
628
633
698
688
646
670
664
605
609
610
692
680
615
616
620
622
694
684
686
627
630
632
634

Fig. 6L

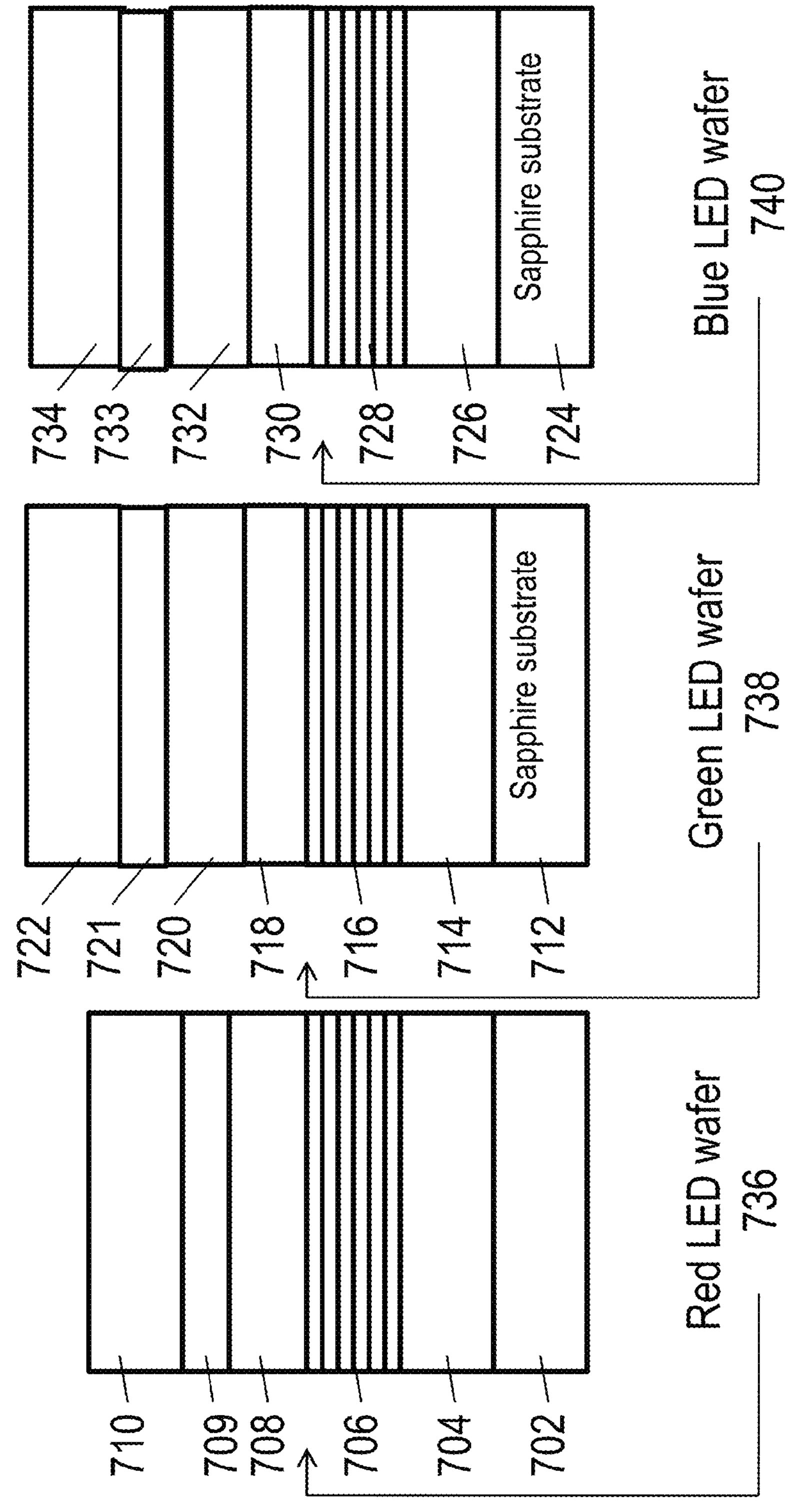

Blue LED wafer
740
Sapphire substrate
734
733
732
730
728
726
724
Green LED wafer
738
Sapphire substrate
722
721
720
718
716
714
712
Red LED wafer
736
710
709
708
706
704
702

Fig. 7A

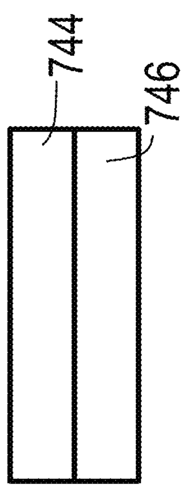


Fig. 7B

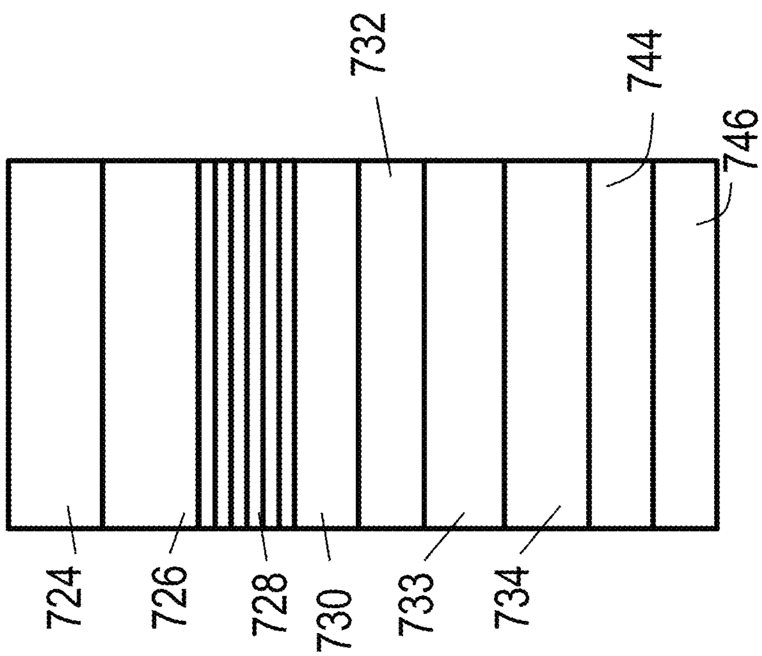


Fig. 7C

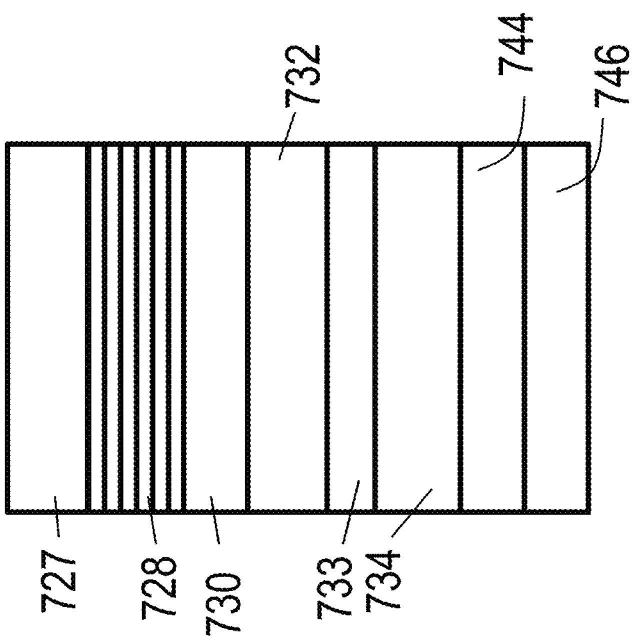


Fig. 7D

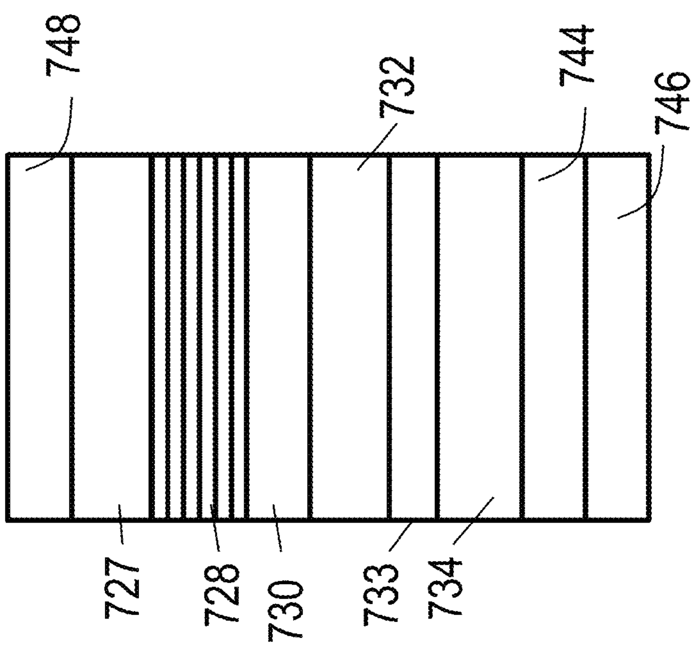


Fig. 7E

Fig. 7F

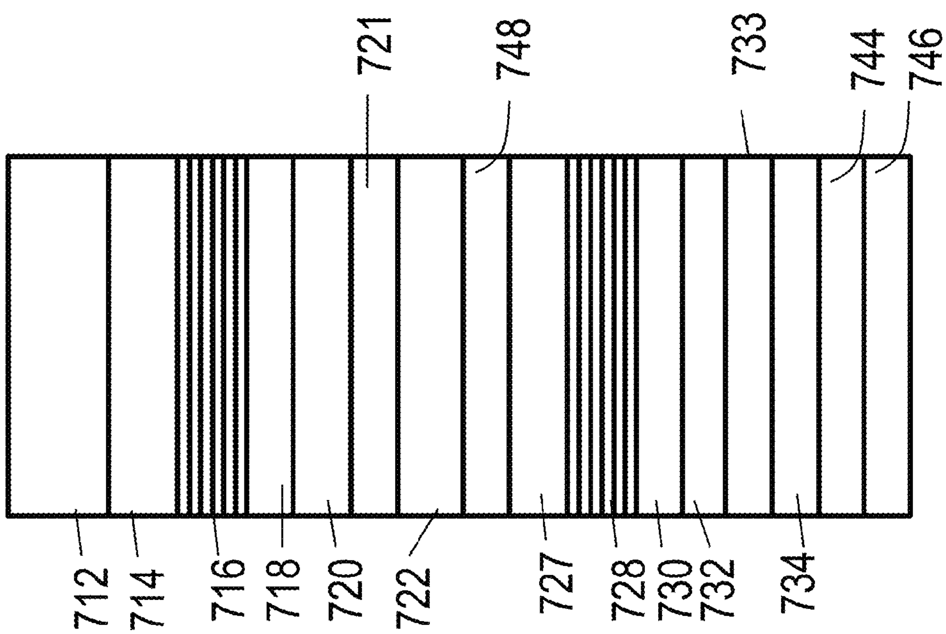


Fig. 7G

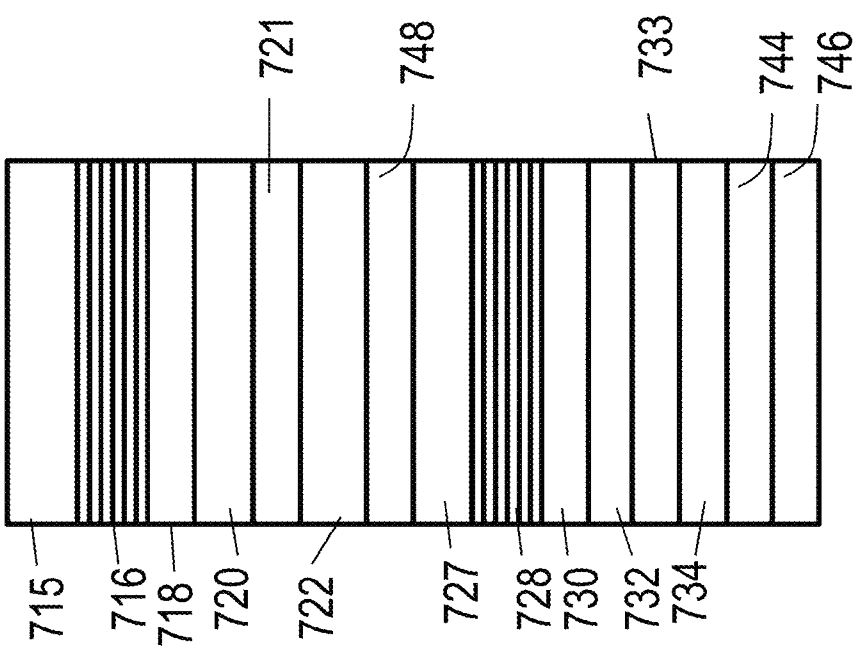


Fig. 7H

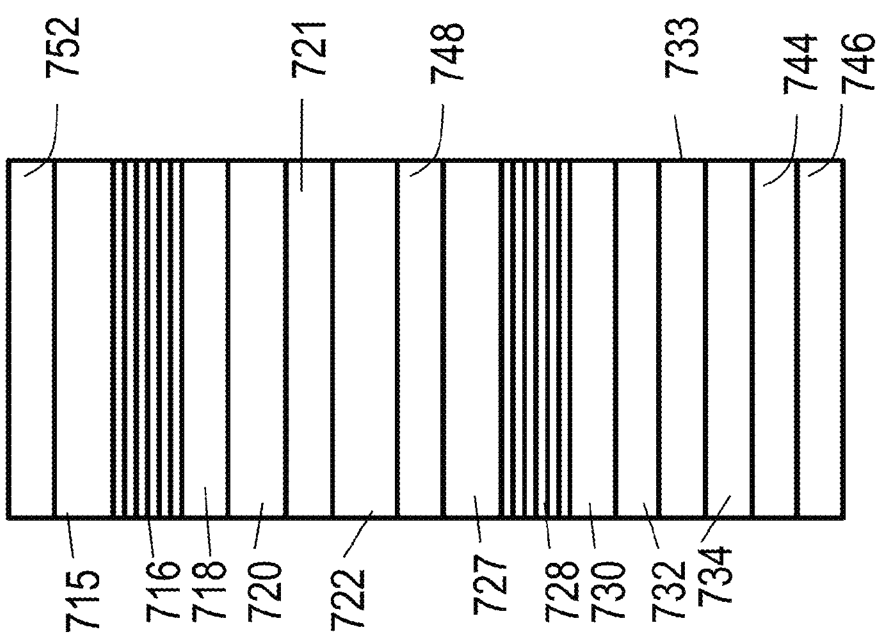


Fig. 7I

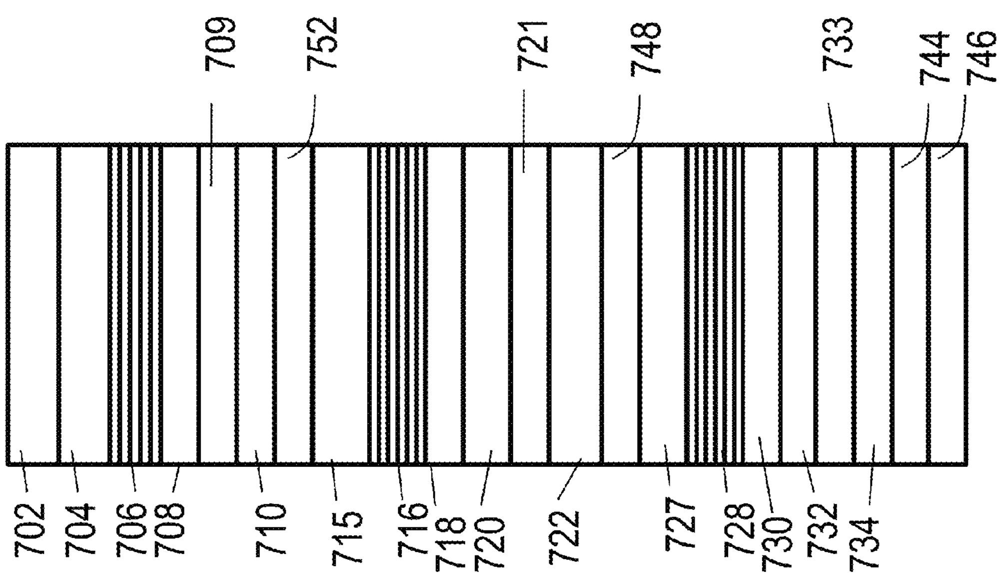
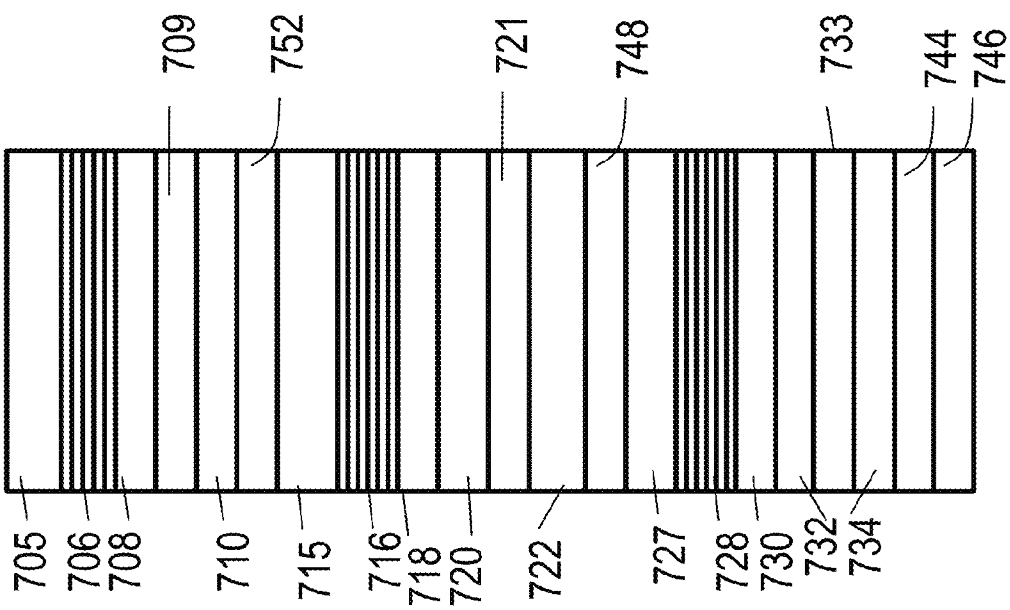
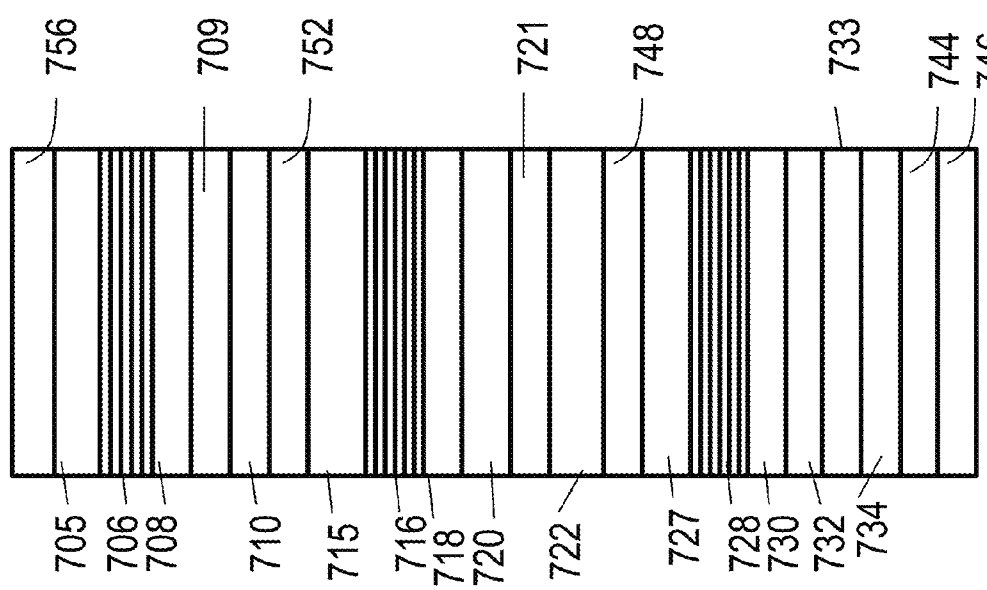

709
752
721
748
733
744
746
702
704
706
708
710
715
716
718
720
722
727
728
730
732
734

Fig. 7J



705
706
708
709
710
715
716
718
720
721
722
727
728
730
732
733
734
744
746
748
752

Fig. 7K


756
709
752
721
748
733
744
746
705
706
708
710
715
716
718
720
722
727
728
730
732
734

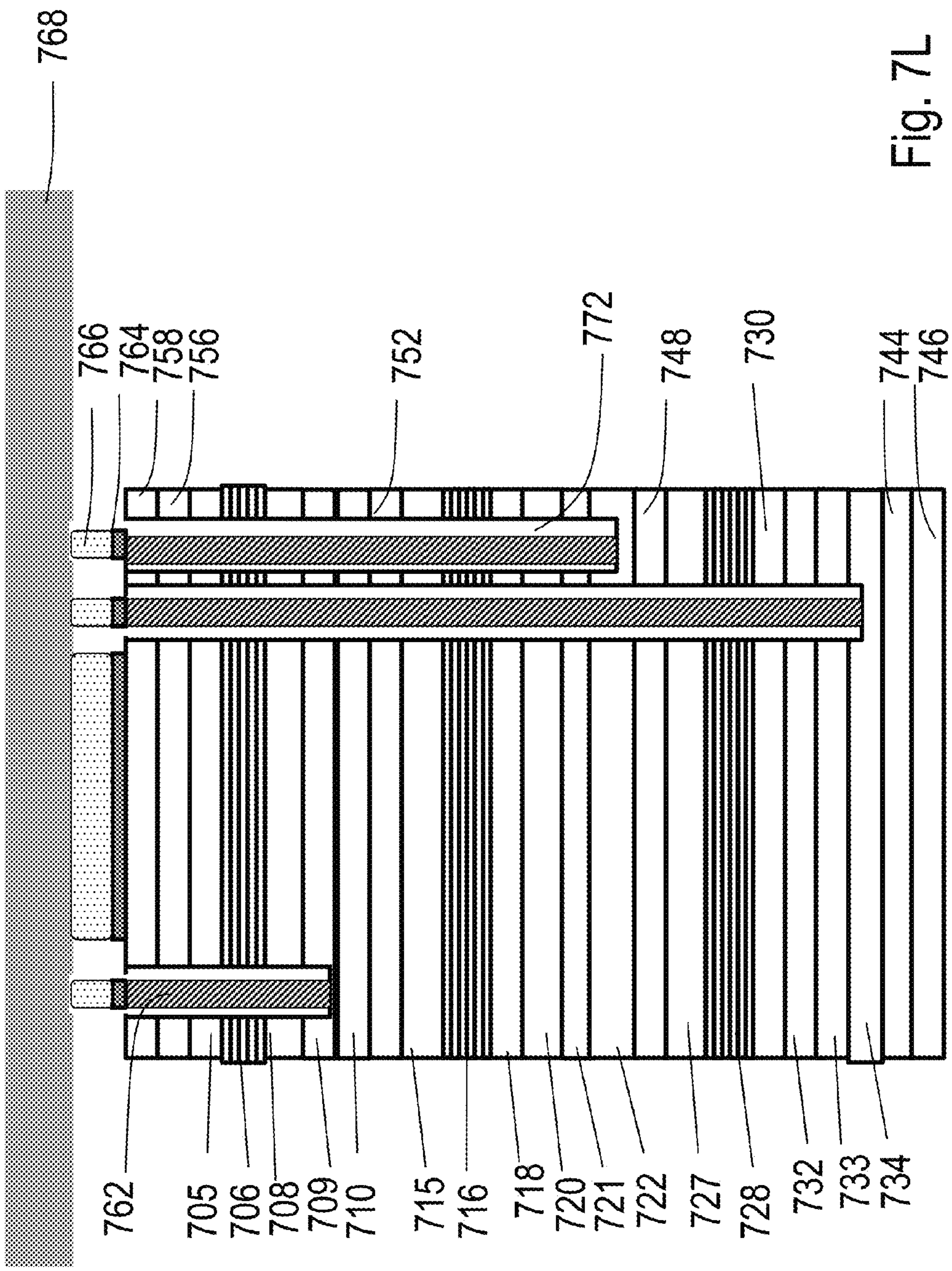
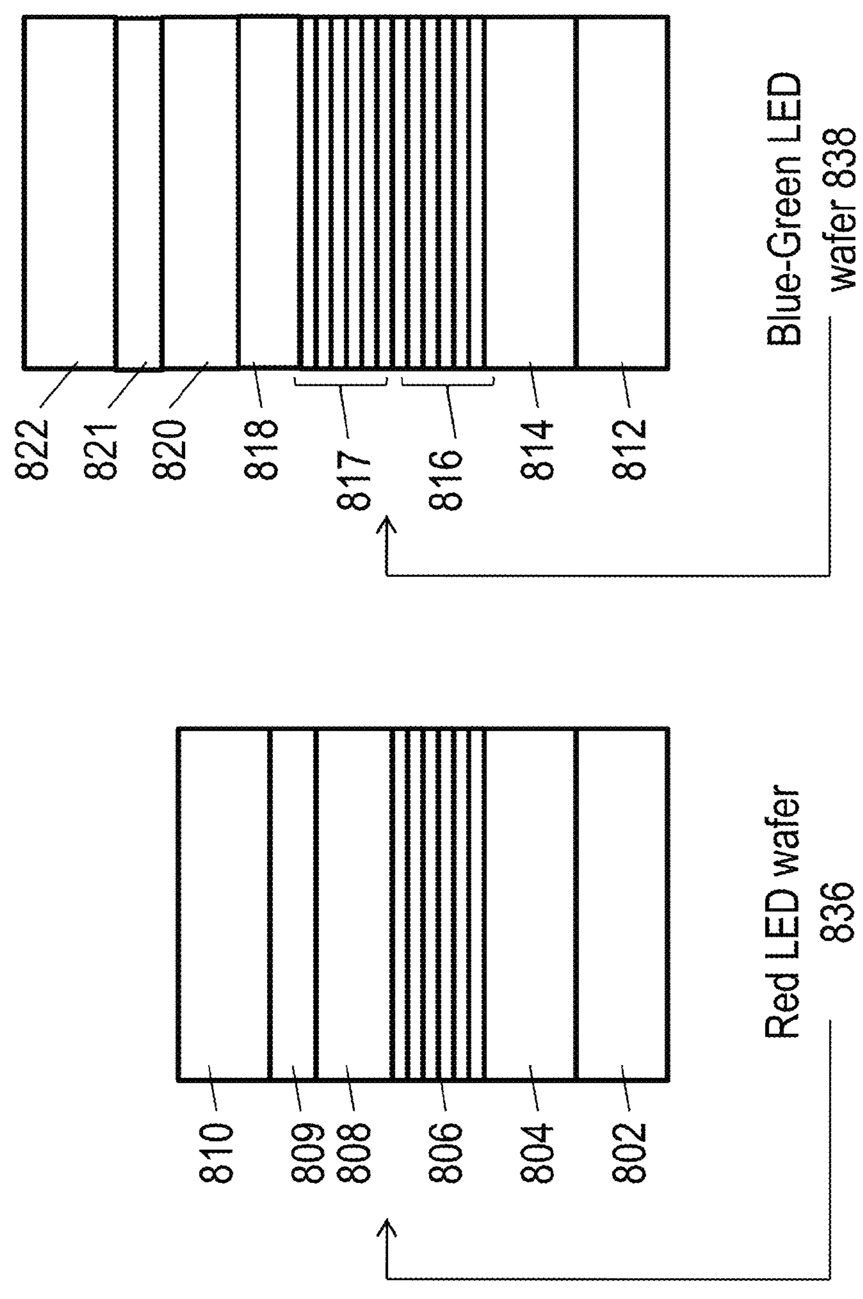

768
766
764
758
756
752
772
748
730
744
746
762
705
706
708
709
710
715
716
718
720
721
722
727
728
732
733
734

Fig. 7L



822
821
820
818
817
816
814
812
Blue-Green LED wafer 838
810
809
808
806
804
802
Red LED wafer 836

Fig. 8A

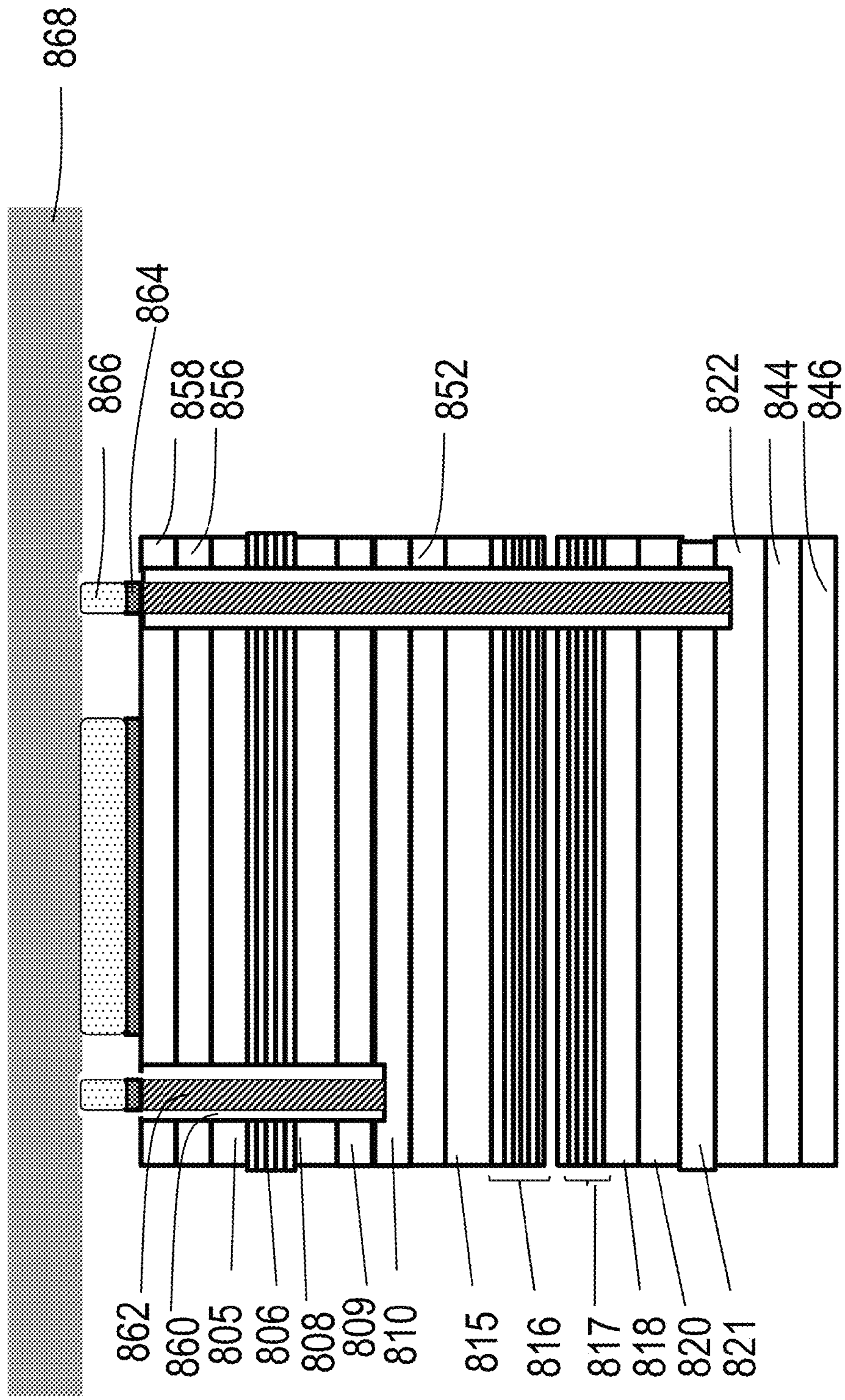

868
866
864
858
856
852
822
844
846
862
860
805
806
808
809
810
815
816
817
818
820
821

Fig. 8B

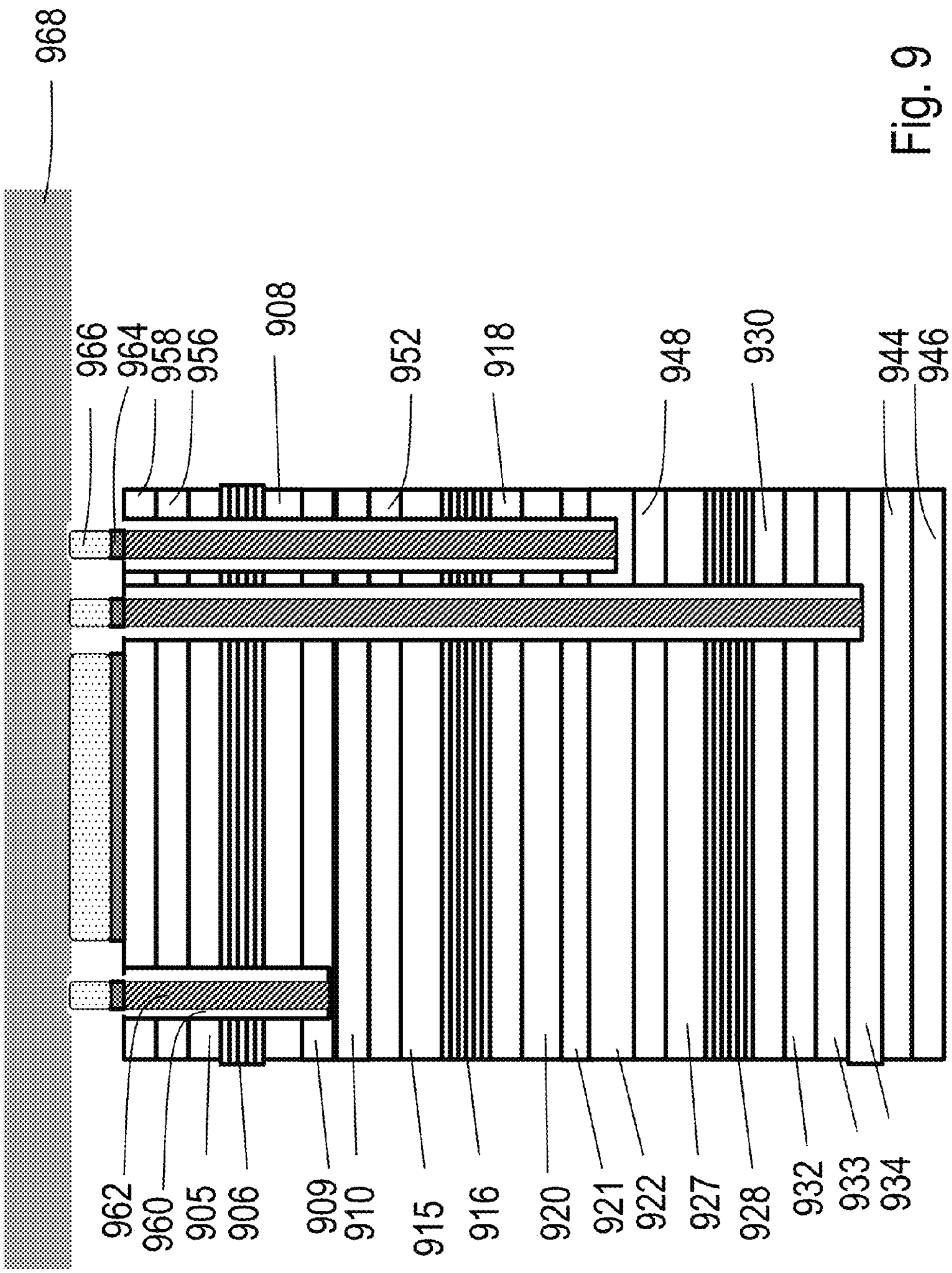
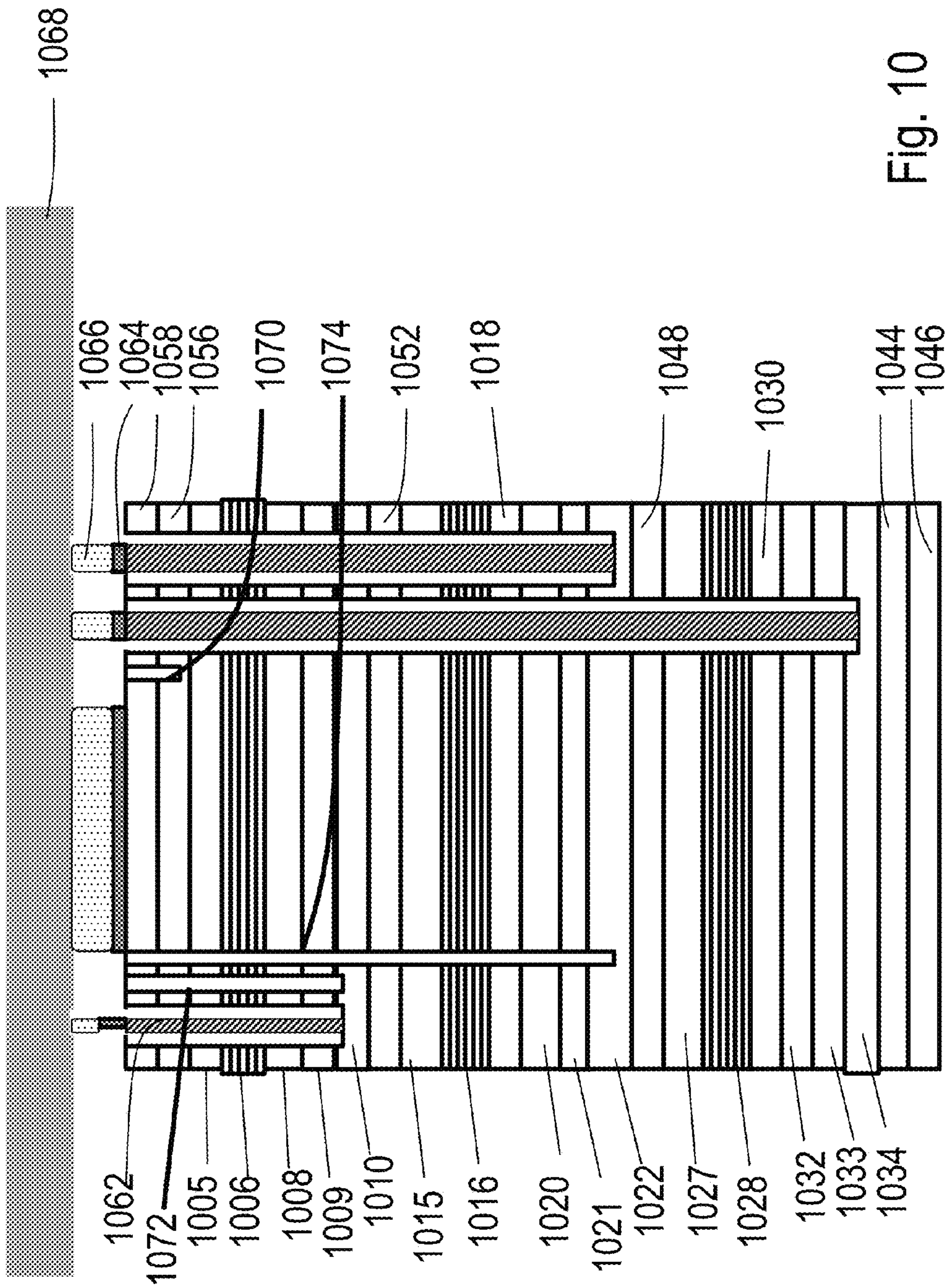

968
966
964
958
956
908
952
918
948
930
944
946
962
960
905
906
909
910
915
916
920
921
922
927
928
932
933
934

Fig. 9



1068
1066
1064
1058
1056
1070
1074
1052
1018
1048
1030
1044
1046
1062
1072
1005
1006
1008
1009
1010
1015
1016
1020
1021
1022
1027
1028
1032
1033
1034

Fig. 10

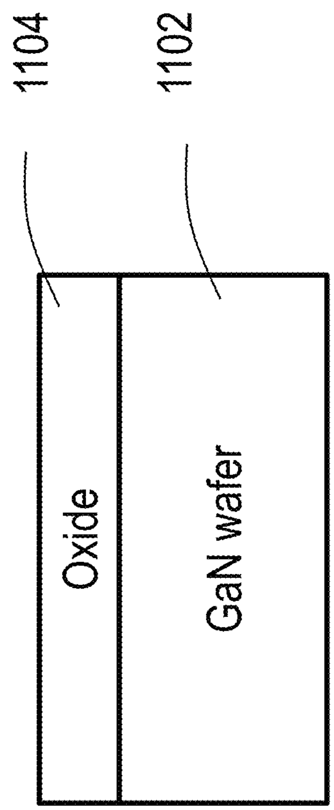


Fig. 11A (Prior art)

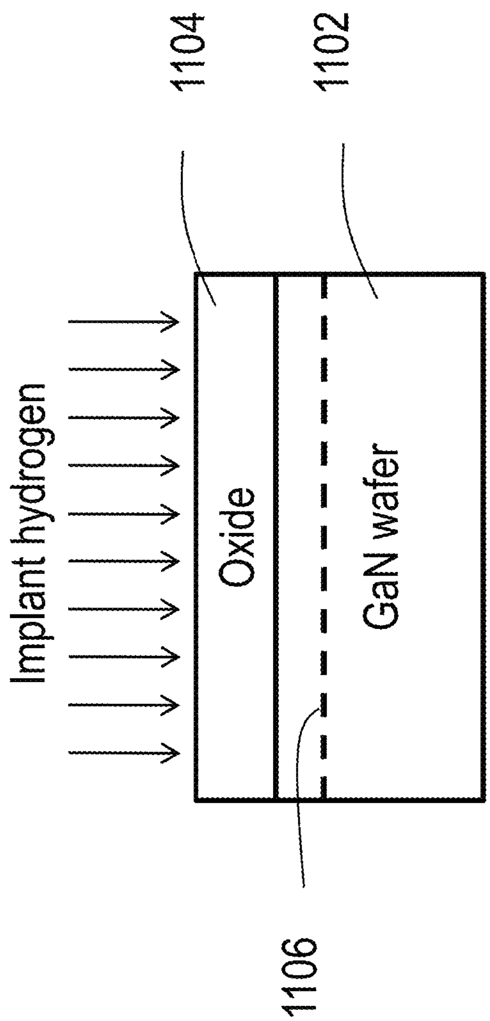


Fig. 11B (Prior art)

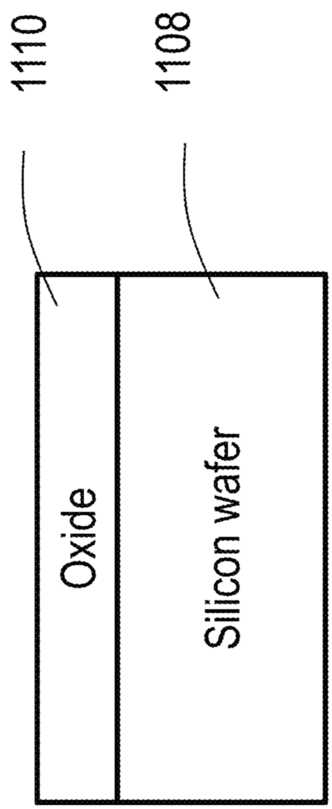


Fig. 11C (Prior art)

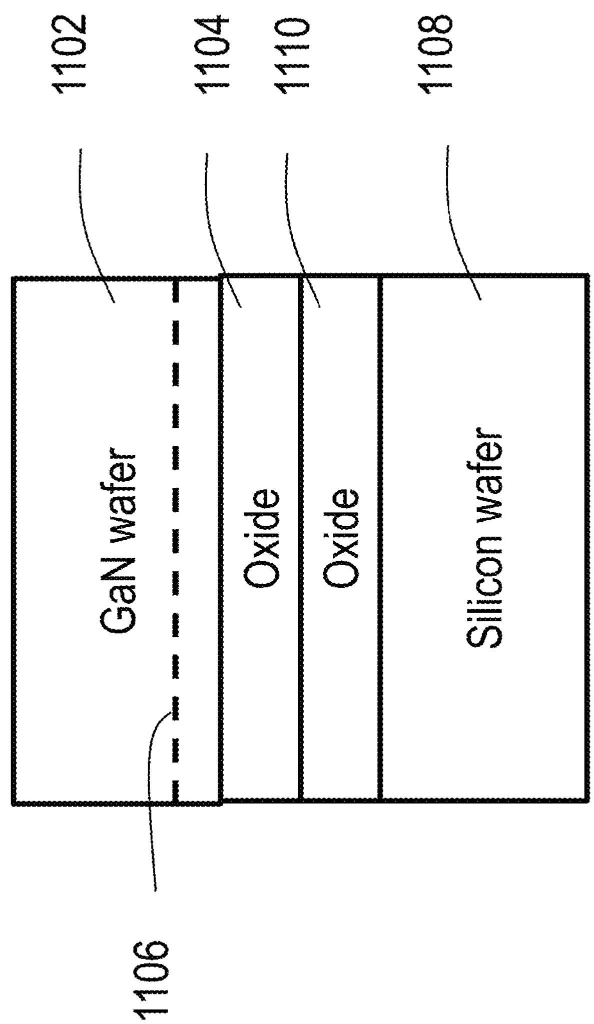


Fig. 11D (Prior art)

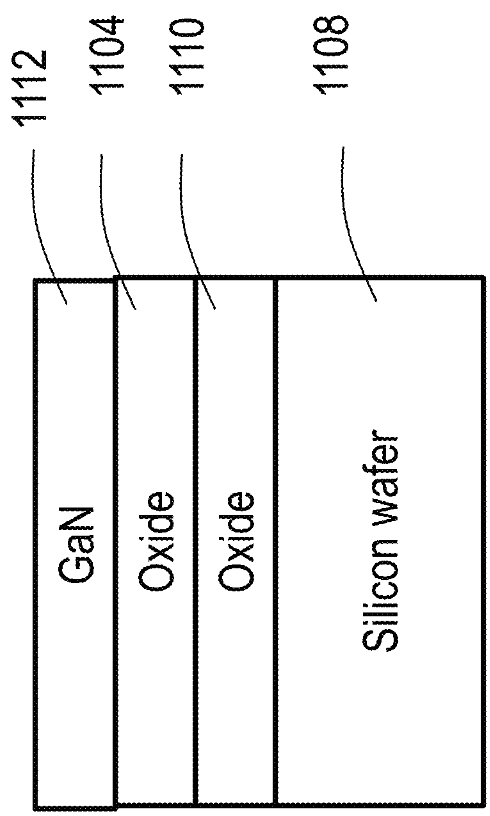


Fig. 11E (Prior art)

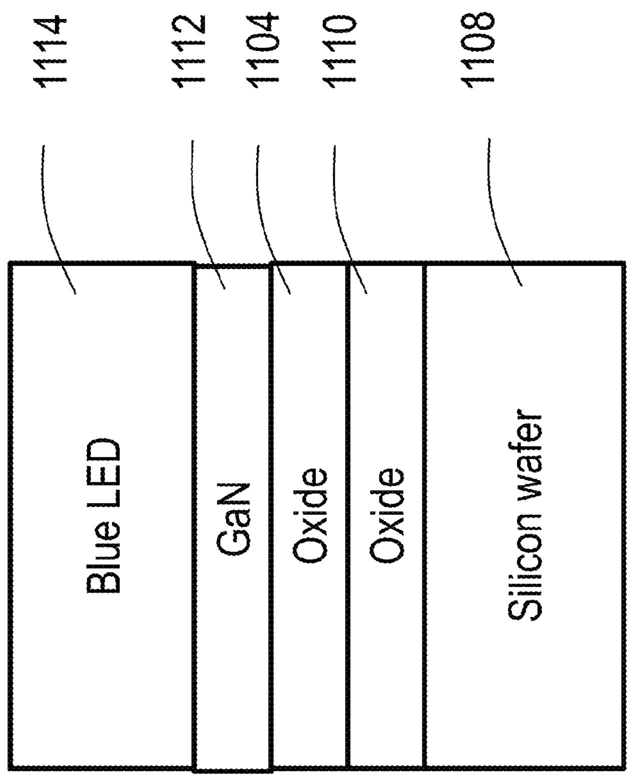


Fig. 11F (Prior art)

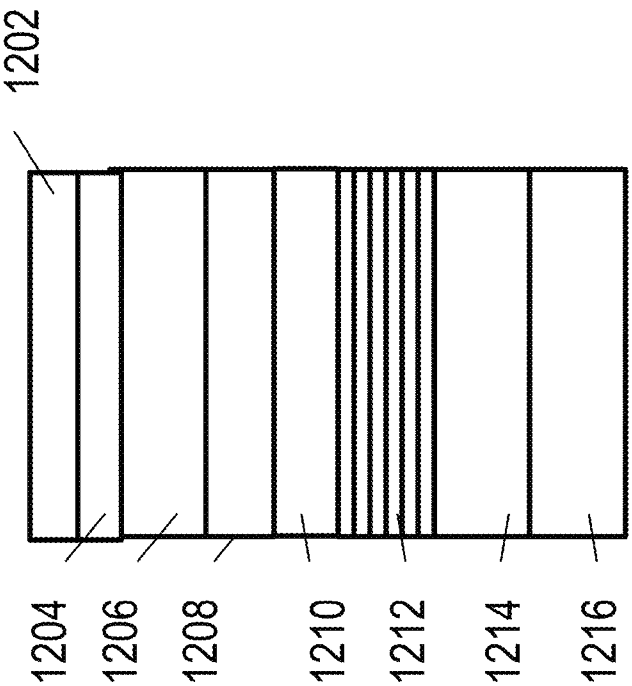


Fig. 12A

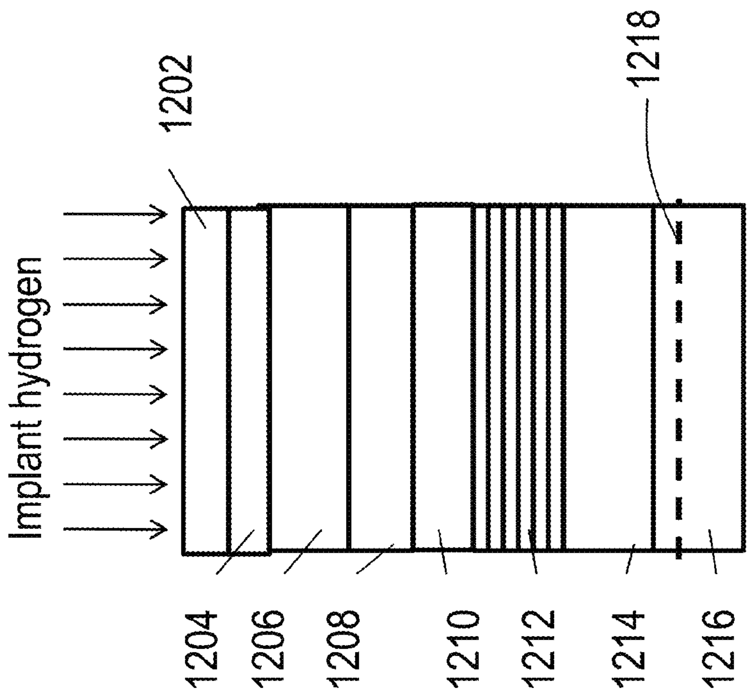

Implant hydrogen
1202
1204
1206
1208
1210
1212
1214
1216
1218

Fig. 12B

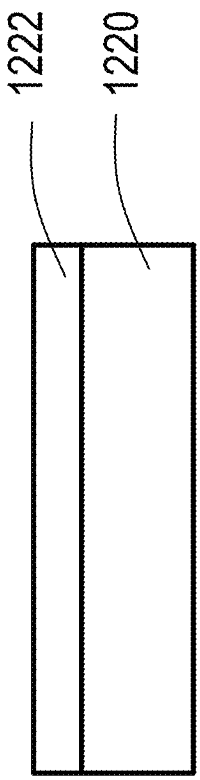


Fig. 12C

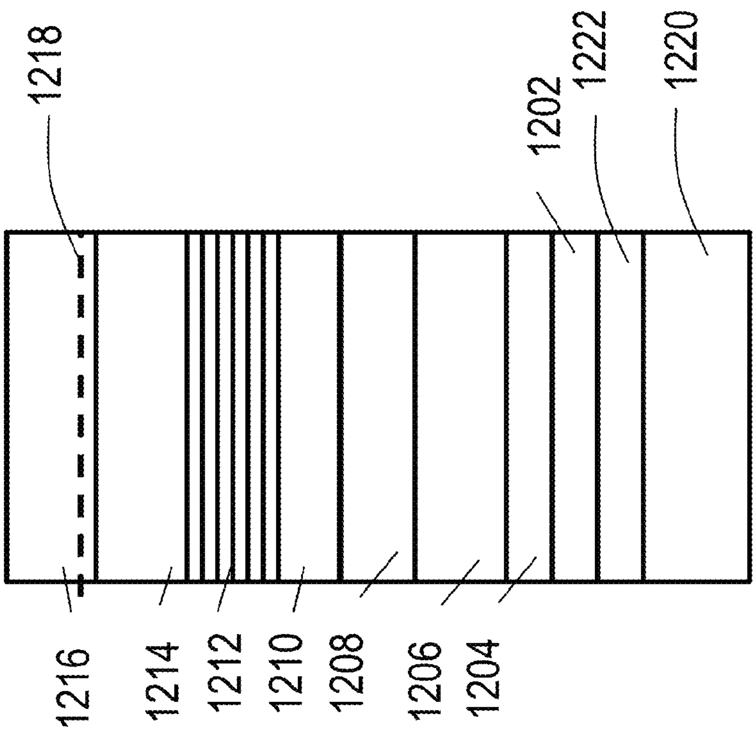


Fig. 12D

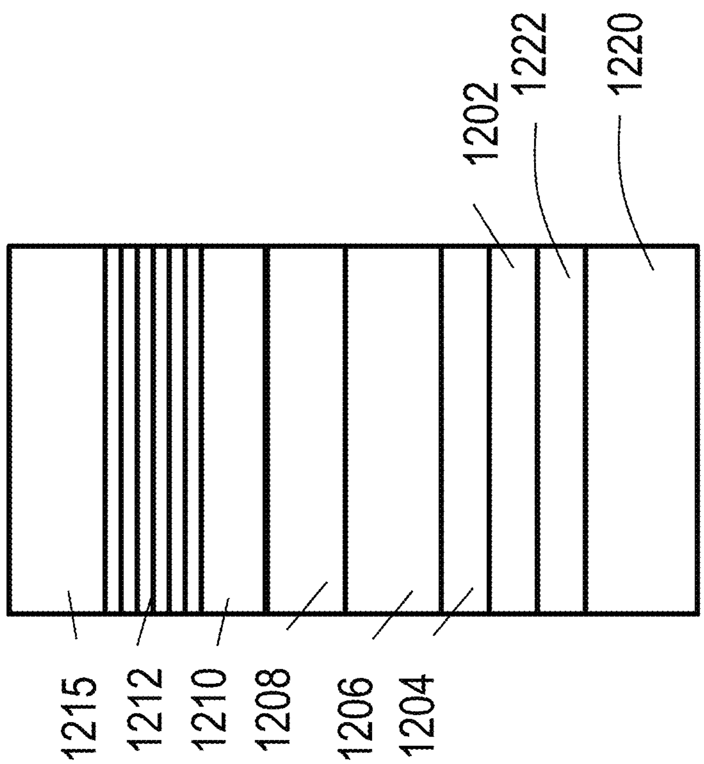


Fig. 12E

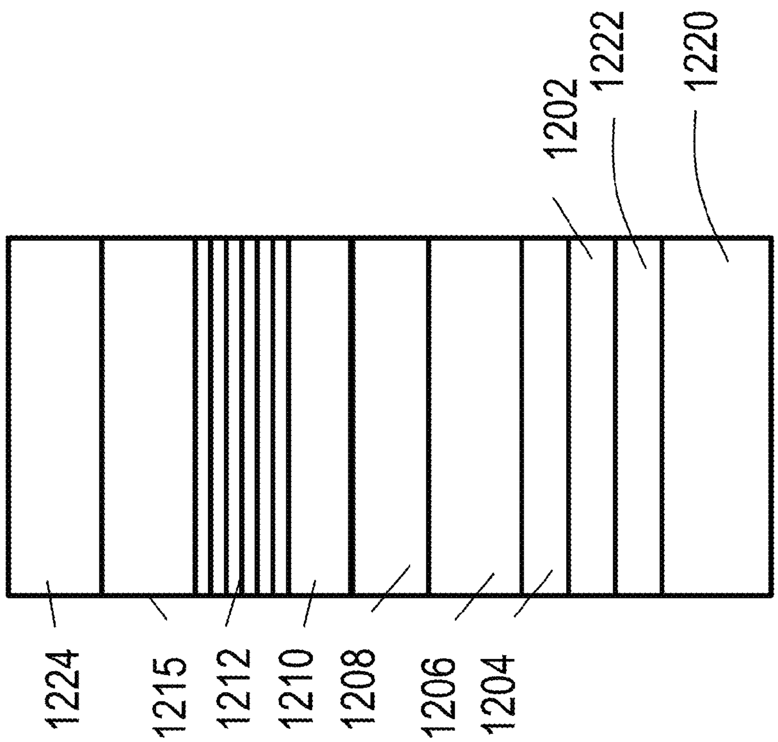


Fig. 12F

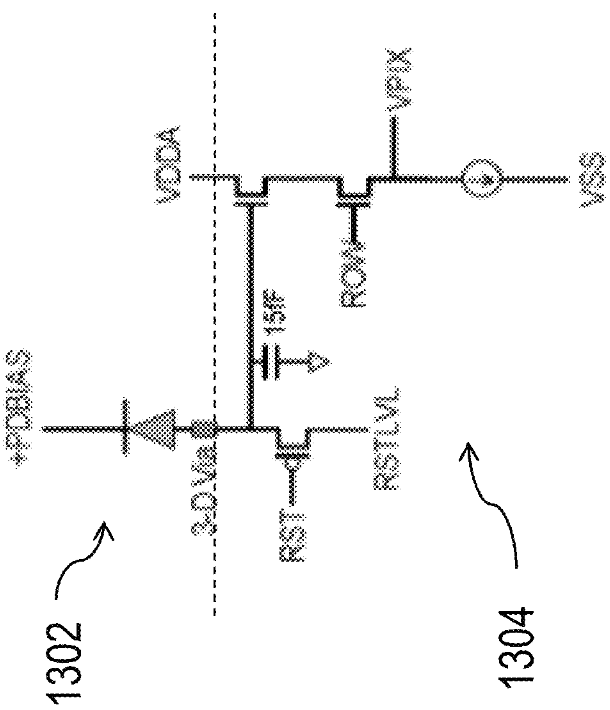


Fig. 13 (Prior art)

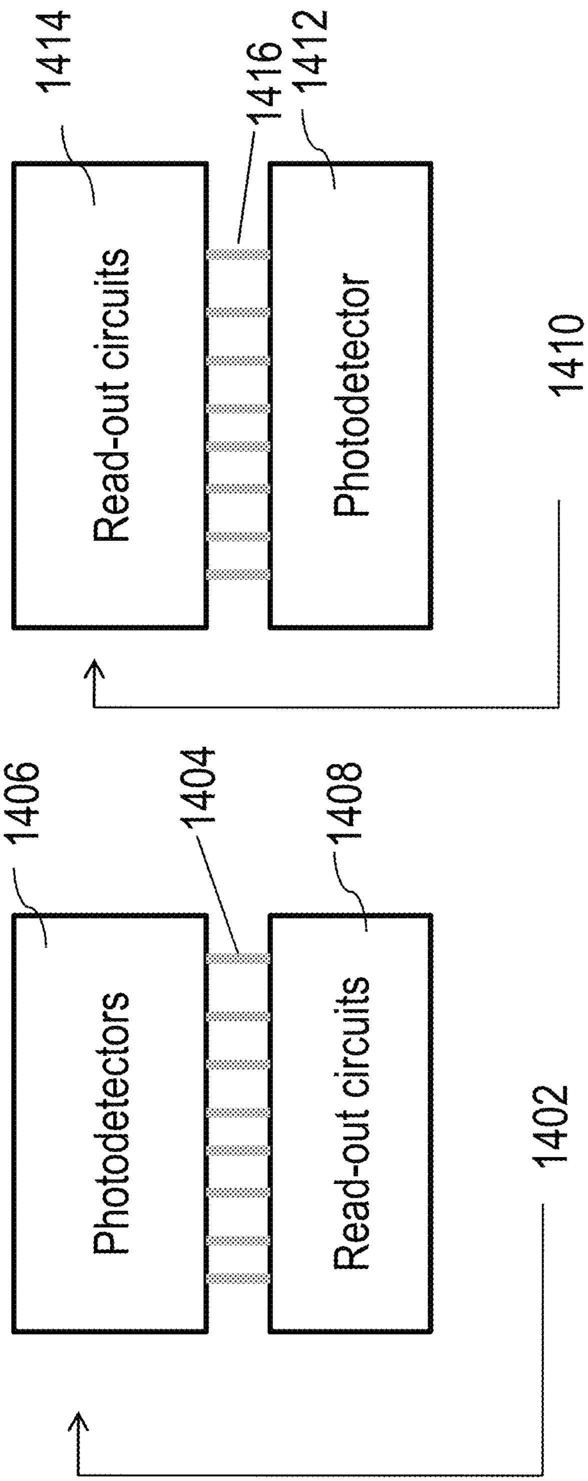

1414
1416
1412
Read-out circuits
Photodetector
1410
1406
1404
1408
Photodetectors
Read-out circuits
1402

Fig. 14

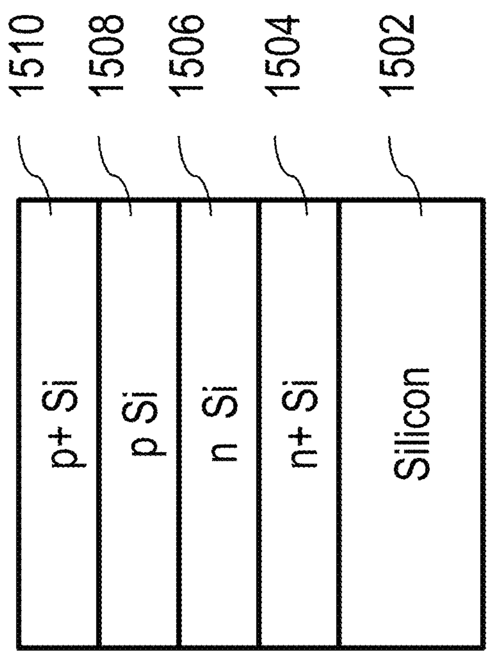


Fig. 15A

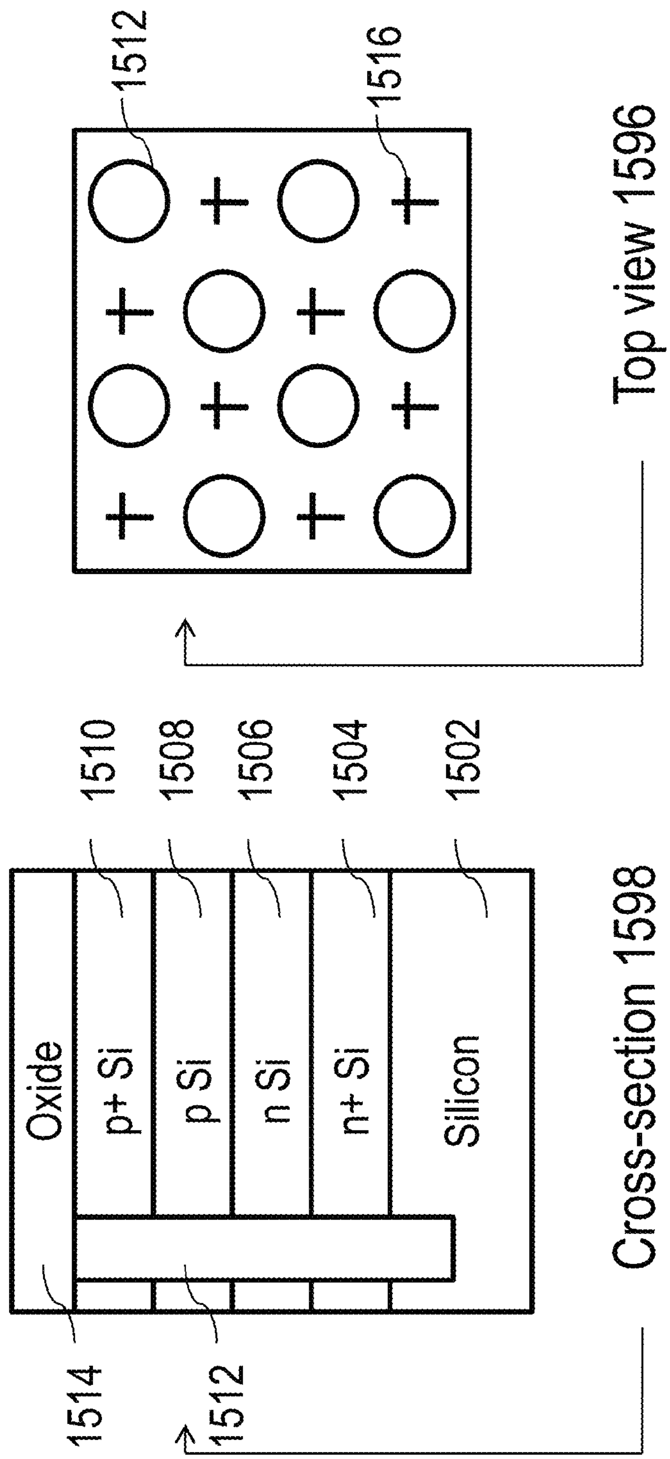

1512
1516
Top view 1596
1510
1508
1506
1504
1502
Oxide
p+ Si
p Si
n Si
n+ Si
Silicon
Cross-section 1598
1514
1512

Fig. 15B

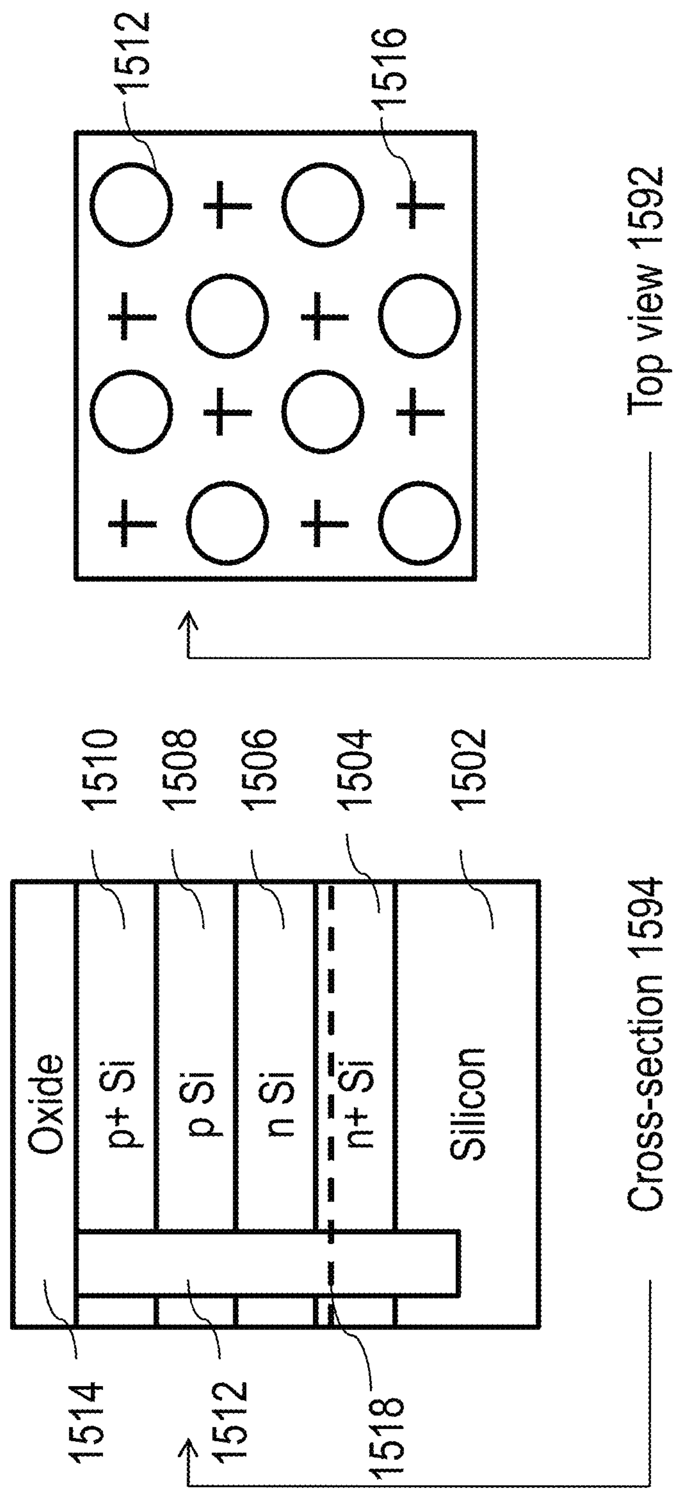

1512
1516
Top view 1592
1510
1508
1506
1504
1502
Oxide
p+ Si
p Si
n Si
n+ Si
Silicon
Cross-section 1594
1514
1512
1518

Fig. 15C

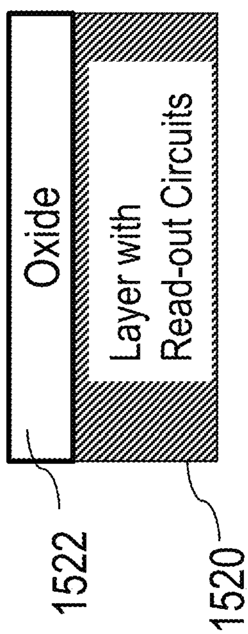


Fig. 15D

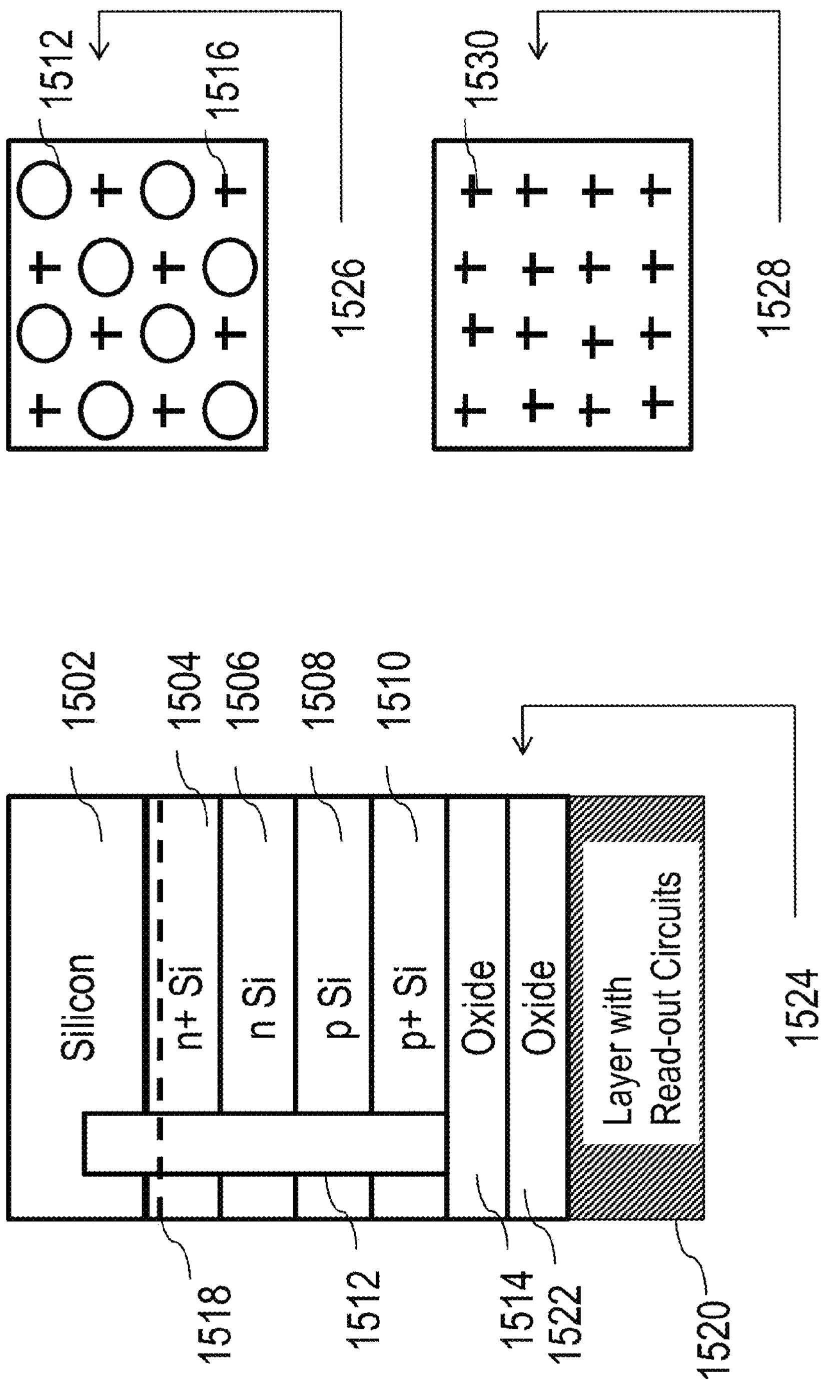

1512
1516
1526
1530
1528
1502
1504
1506
1508
1510
Silicon
n+ Si
n Si
p Si
p+ Si
Oxide
Oxide
Layer with
Read-out Circuits
1524
1518
1512
1514
1522
1520

Fig. 15E

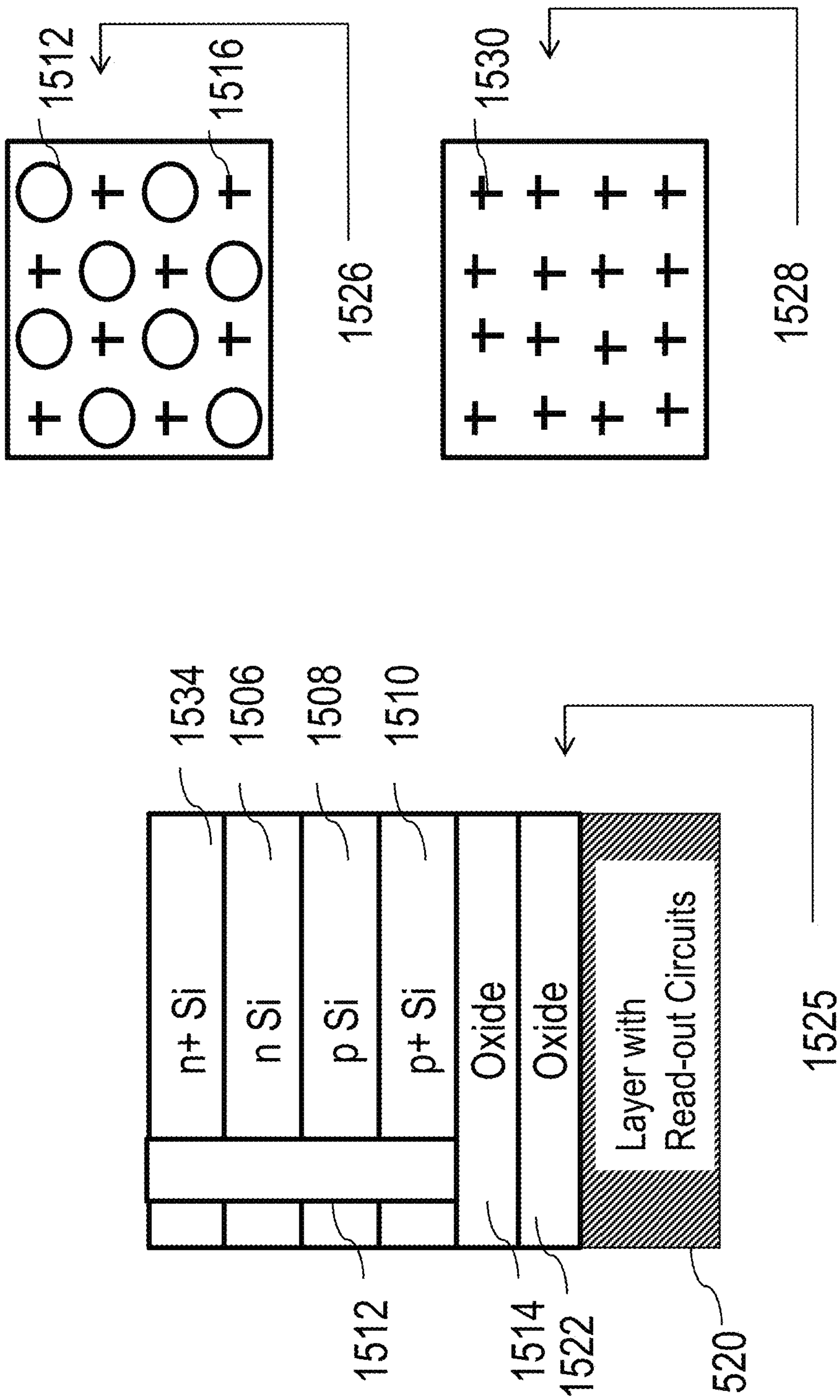

1512
1516
1526
1530
1528
1534
1506
1508
1510
n+ Si
n Si
p Si
p+ Si
Oxide
Oxide
Layer with
Read-out Circuits
1525
1512
1514
1522
1520

Fig. 15F

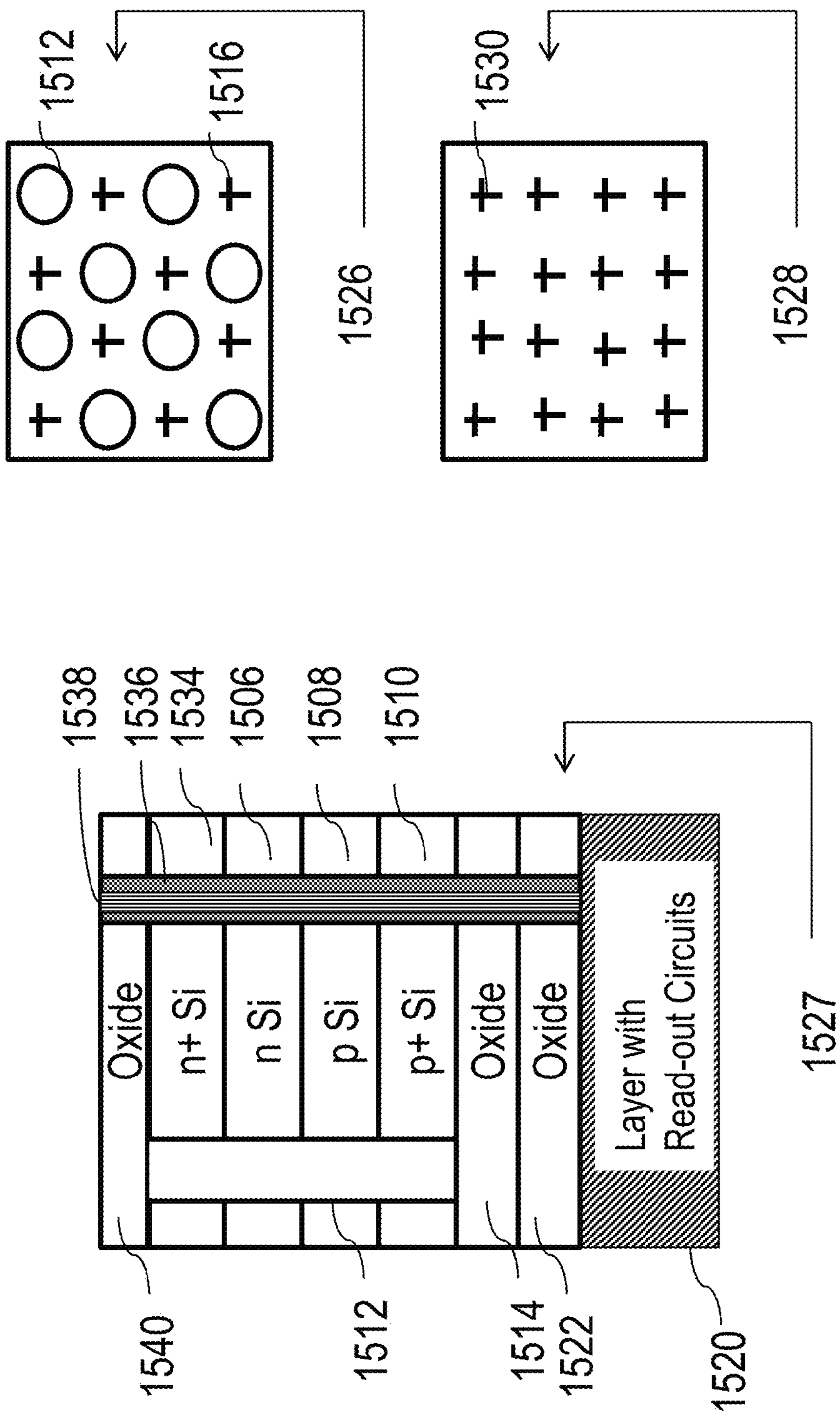
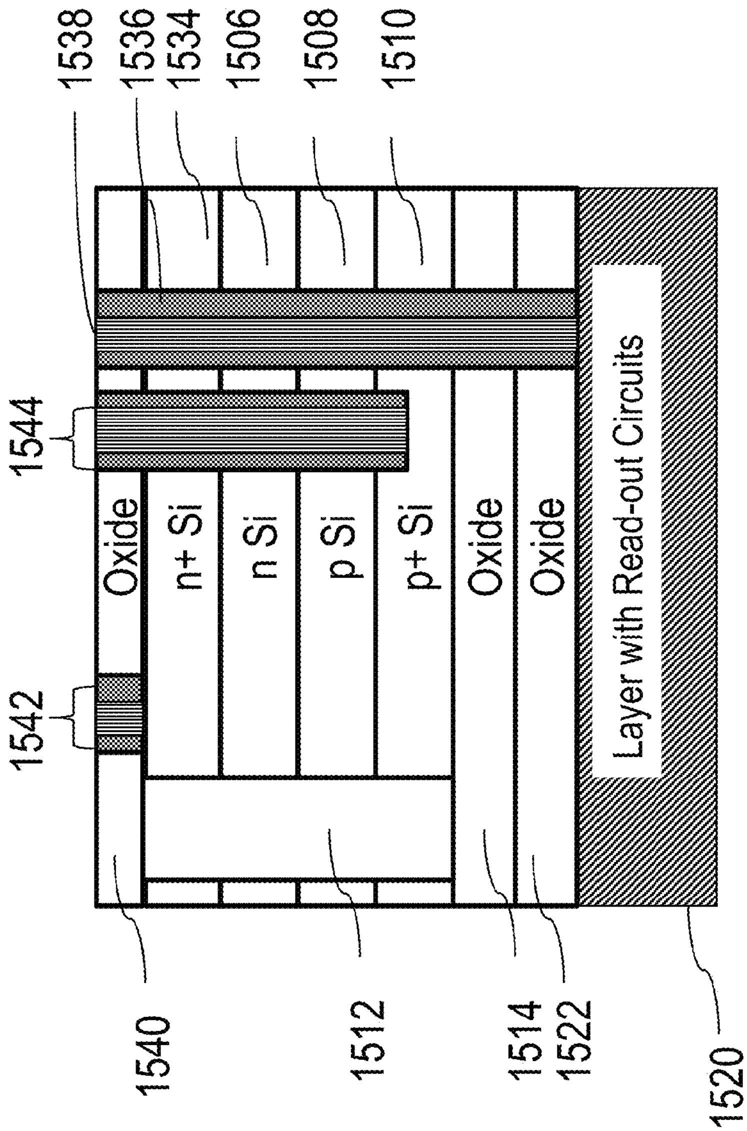

1512
1516
1526
1530
1528
1538
1536
1534
1506
1508
1510
Oxide
n+ Si
n Si
p Si
p+ Si
Oxide
Oxide
Layer with
Read-out Circuits
1527
1540
1512
1514
1522
1520

Fig. 15G



1538
1536
1534
1506
1508
1510
1544
1542
Oxide
n+ Si
n Si
p Si
p+ Si
Oxide
Oxide
Layer with Read-out Circuits
1540
1512
1514
1522
1520

Fig. 15H

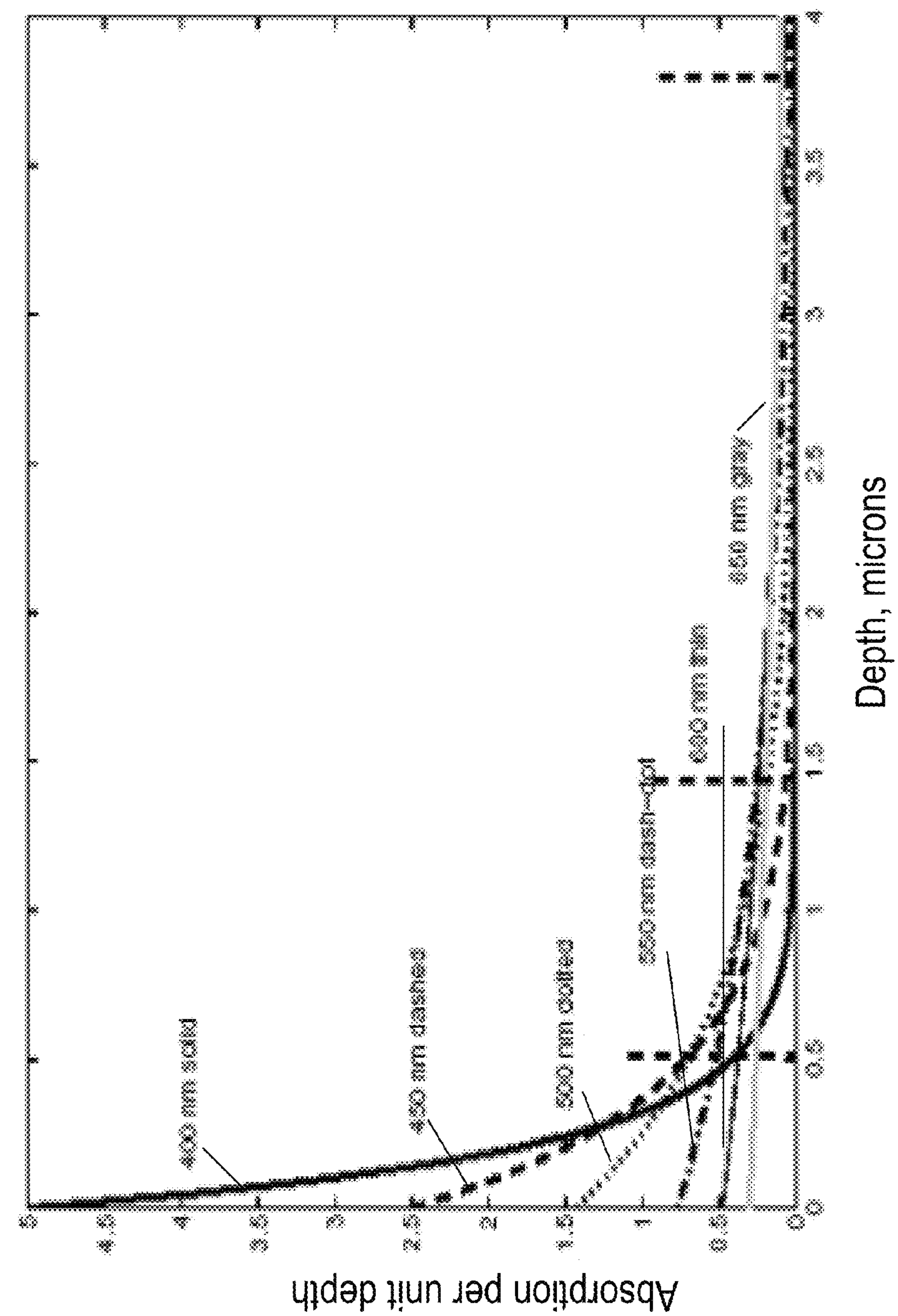

400 nm solid
450 nm dashed
500 nm dotted
550 nm dash-dot
650 nm thin
850 nm gray
Depth, microns
Absorption per unit depth
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5

Fig. 16

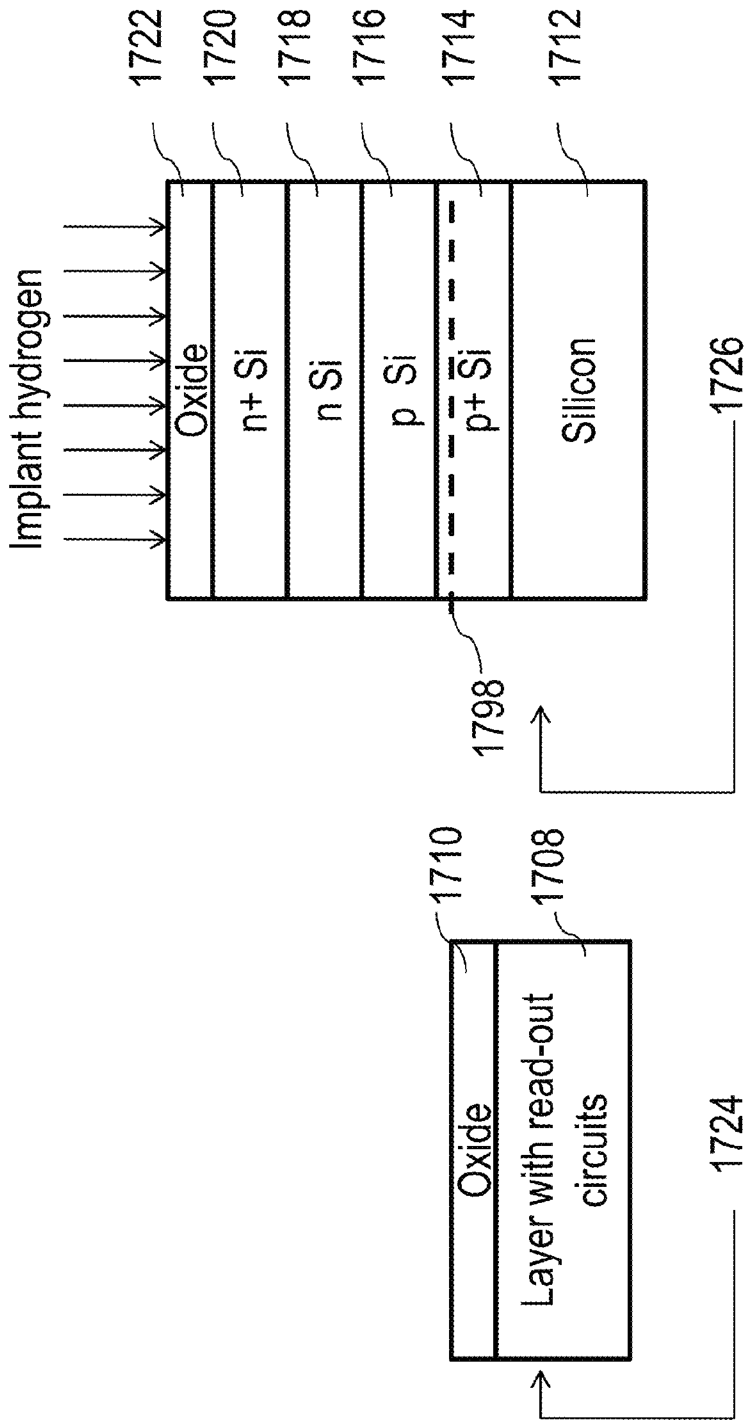
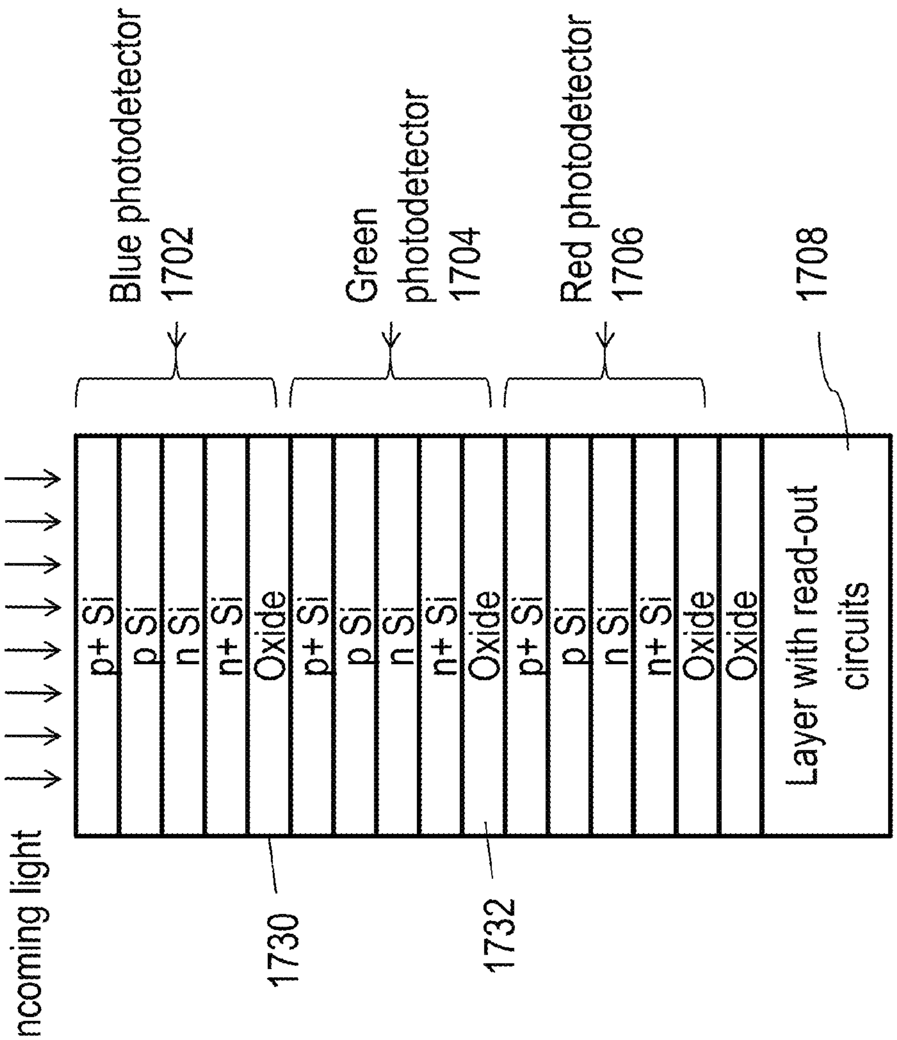
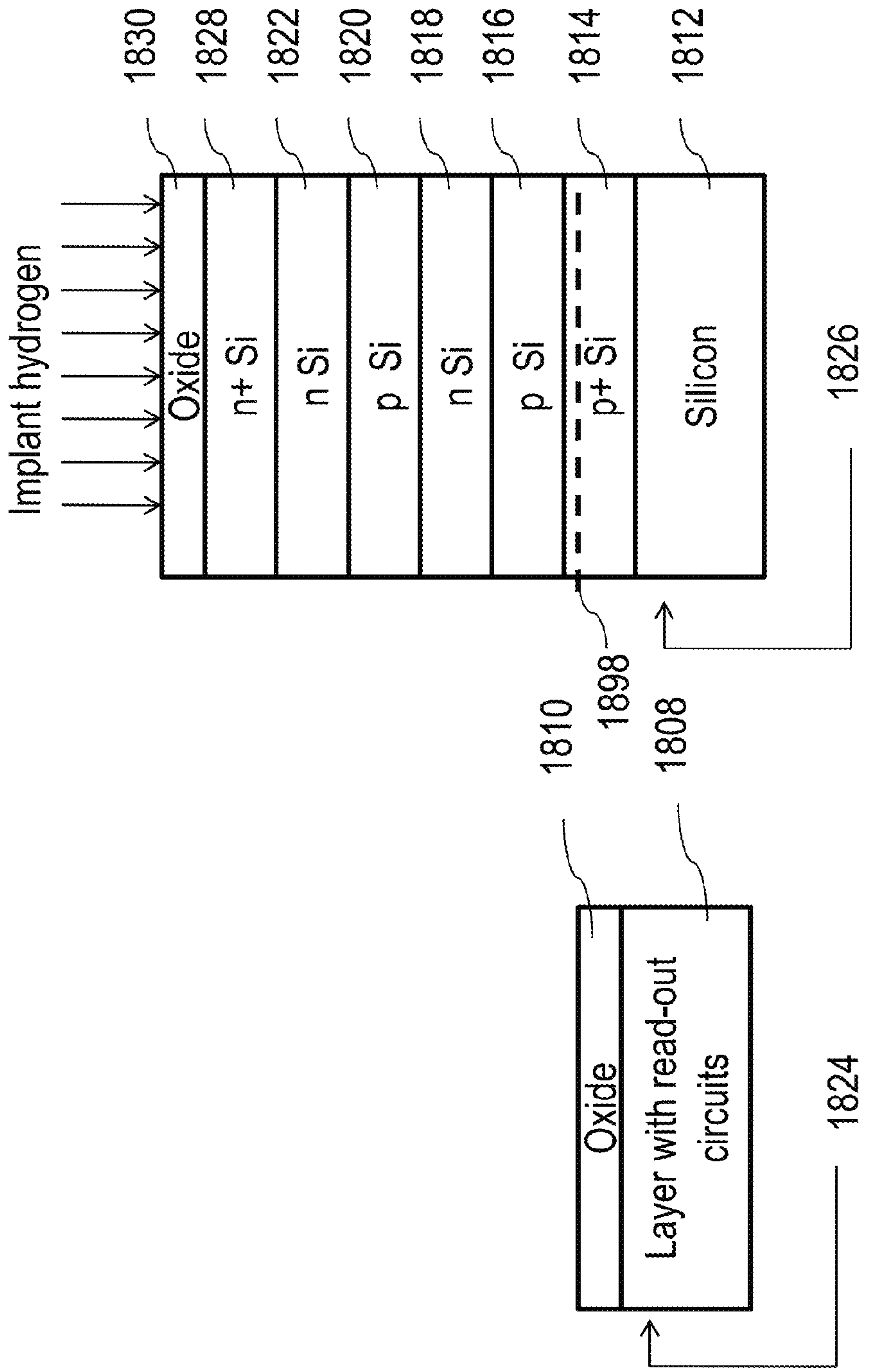

1722
1720
1718
1716
1714
1712
Implant hydrogen
Oxide
n+ Si
n Si
p Si
p+ Si
Silicon
1726
1798
1710
1708
Oxide
Layer with read-out circuits
1724

Fig. 17A



Incoming light
Blue photodetector
1702
Green
photodetector
1704
Red photodetector
1706
1708
p+ Si
p Si
n Si
n+ Si
Oxide
p+ Si
p Si
n Si
n+ Si
Oxide
p+ Si
p Si
n Si
n+ Si
Oxide
Oxide
Layer with read-out
circuits
1730
1732

Fig. 17B



Implant hydrogen
Oxide
n+ Si
n Si
p Si
n Si
p Si
p+ Si
Silicon
1830
1828
1822
1820
1818
1816
1814
1812
1826
1898
1810
1808
Oxide
Layer with read-out circuits
1824

Fig. 18A

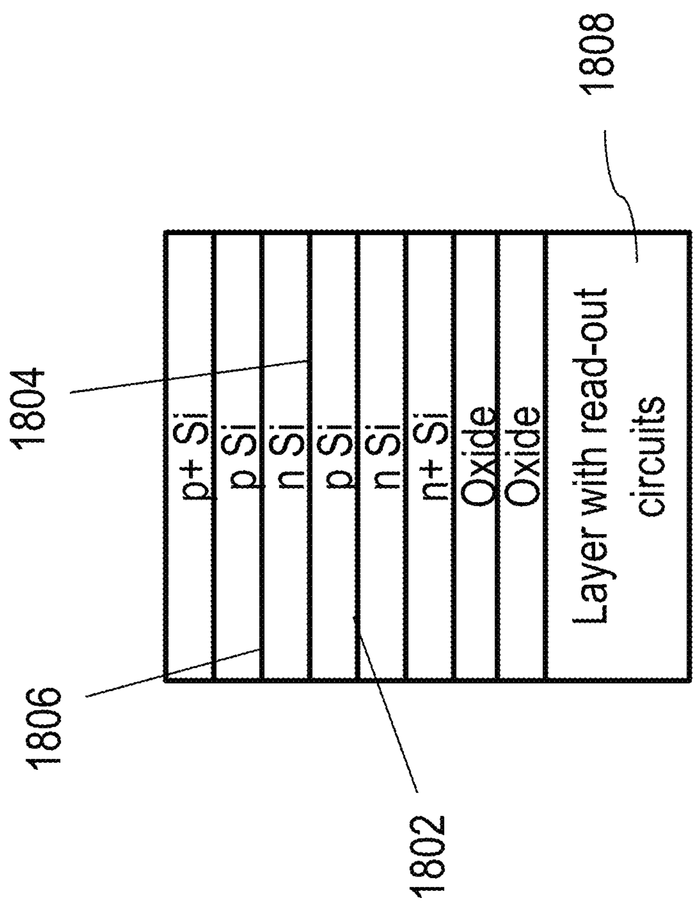

1808
1804
p+ Si
p Si
n Si
p Si
n Si
n+ Si
Oxide
Oxide
Layer with read-out circuits
1806
1802

Fig. 18B

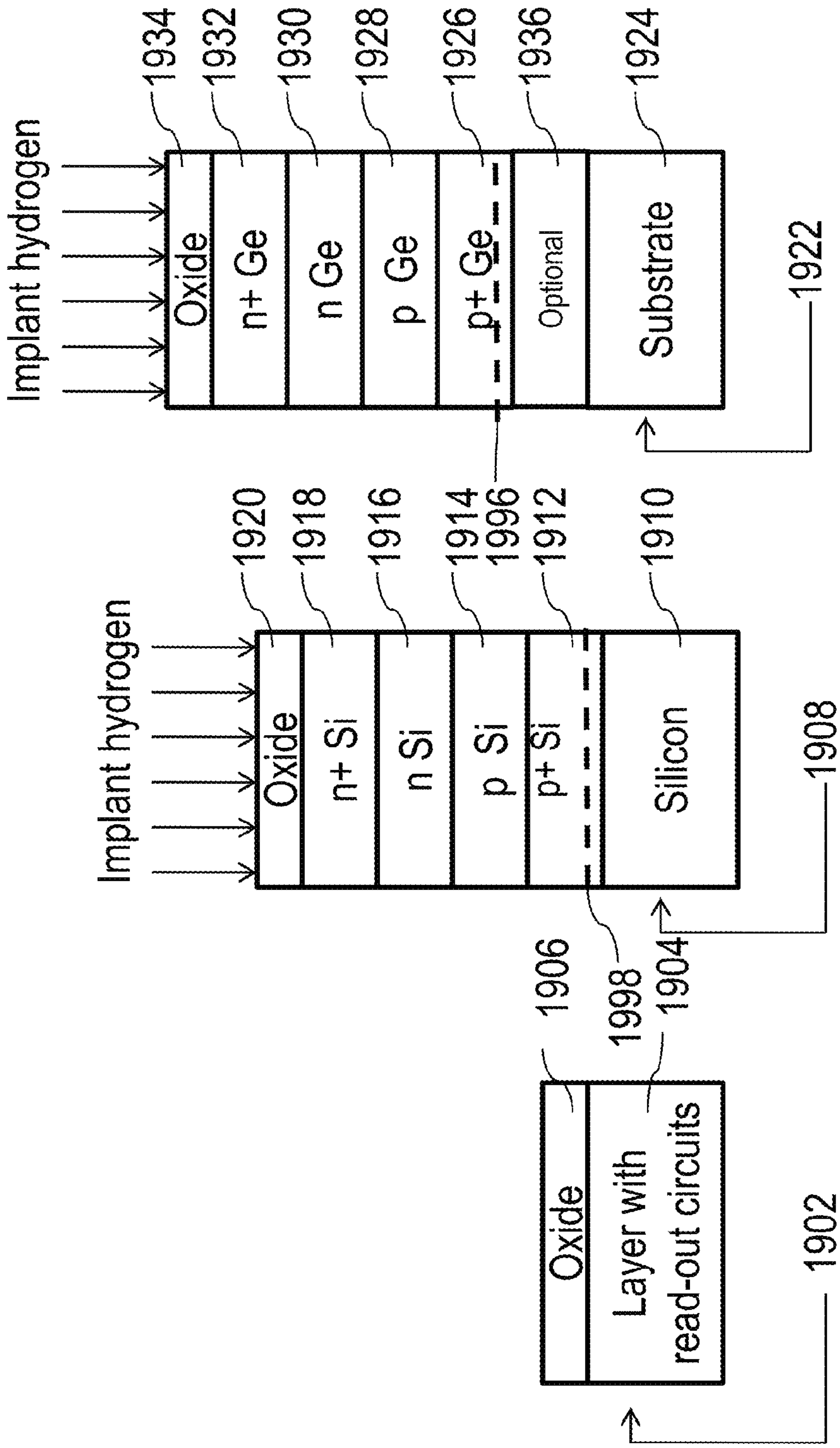

Implant hydrogen
Oxide
n+ Ge
n Ge
p Ge
p+ Ge
Optional
Substrate
1934
1932
1930
1928
1926
1936
1924
1922
1996
Implant hydrogen
Oxide
n+ Si
n Si
p Si
p+ Si
Silicon
1920
1918
1916
1914
1912
1910
1908
1998
1904
1906
Oxide
Layer with
read-out circuits
1902

Fig. 19A

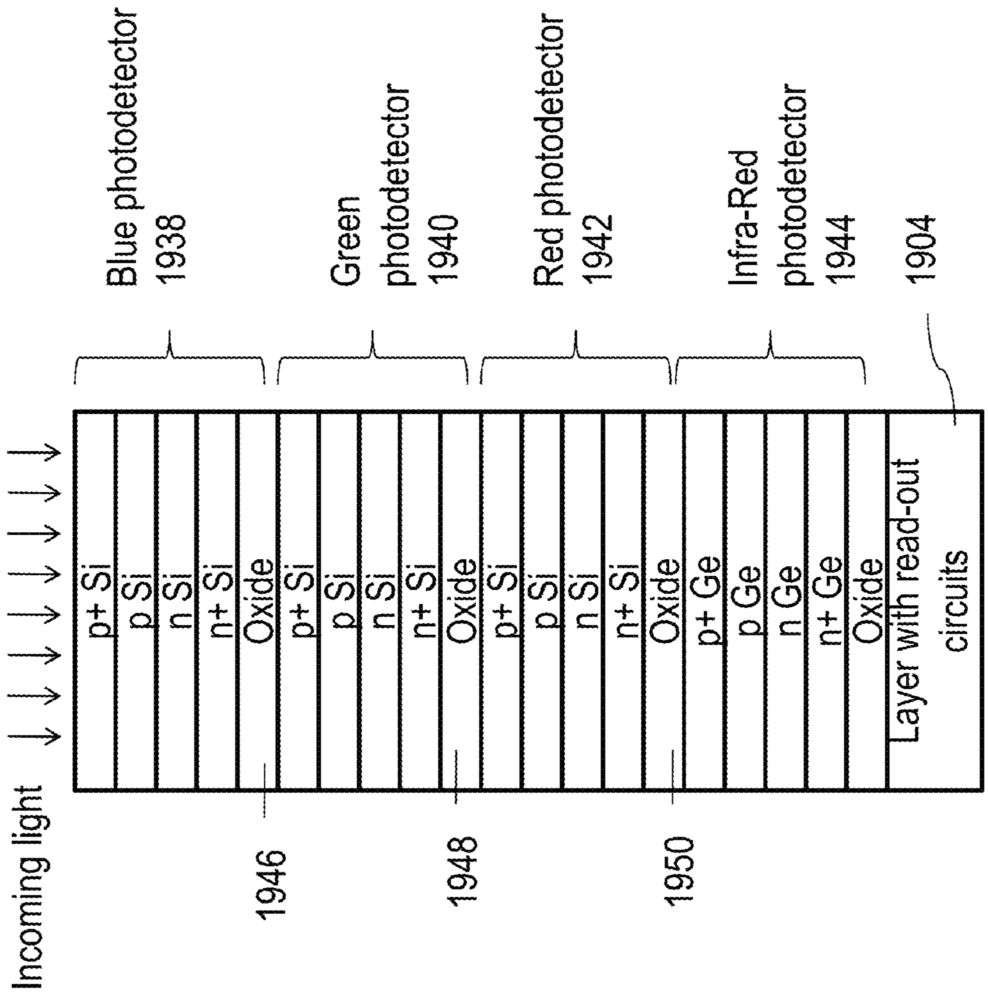

Incoming light
Blue photodetector
1938
Green
photodetector
1940
Red photodetector
1942
Infra-Red
photodetector
1944
1904
p+ Si
p Si
n Si
n+ Si
Oxide
p+ Si
p Si
n Si
n+ Si
Oxide
p+ Si
p Si
n Si
n+ Si
Oxide
p+ Ge
p Ge
n Ge
n+ Ge
Oxide
Layer with read-out
circuits
1946
1948
1950

Fig. 19B

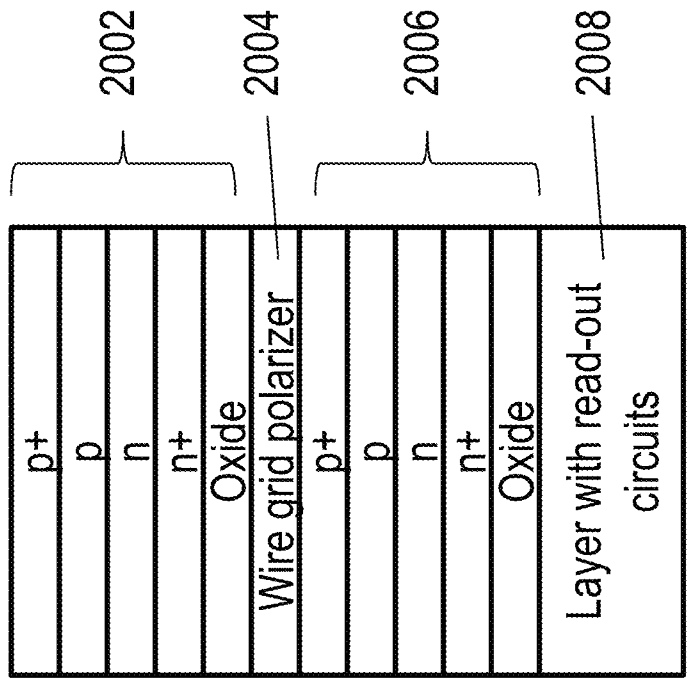

2002
2004
2006
2008
p+
p
n
n+
Oxide
Wire grid polarizer
p+
p
n
n+
Oxide
Layer with read-out circuits

Fig. 20A

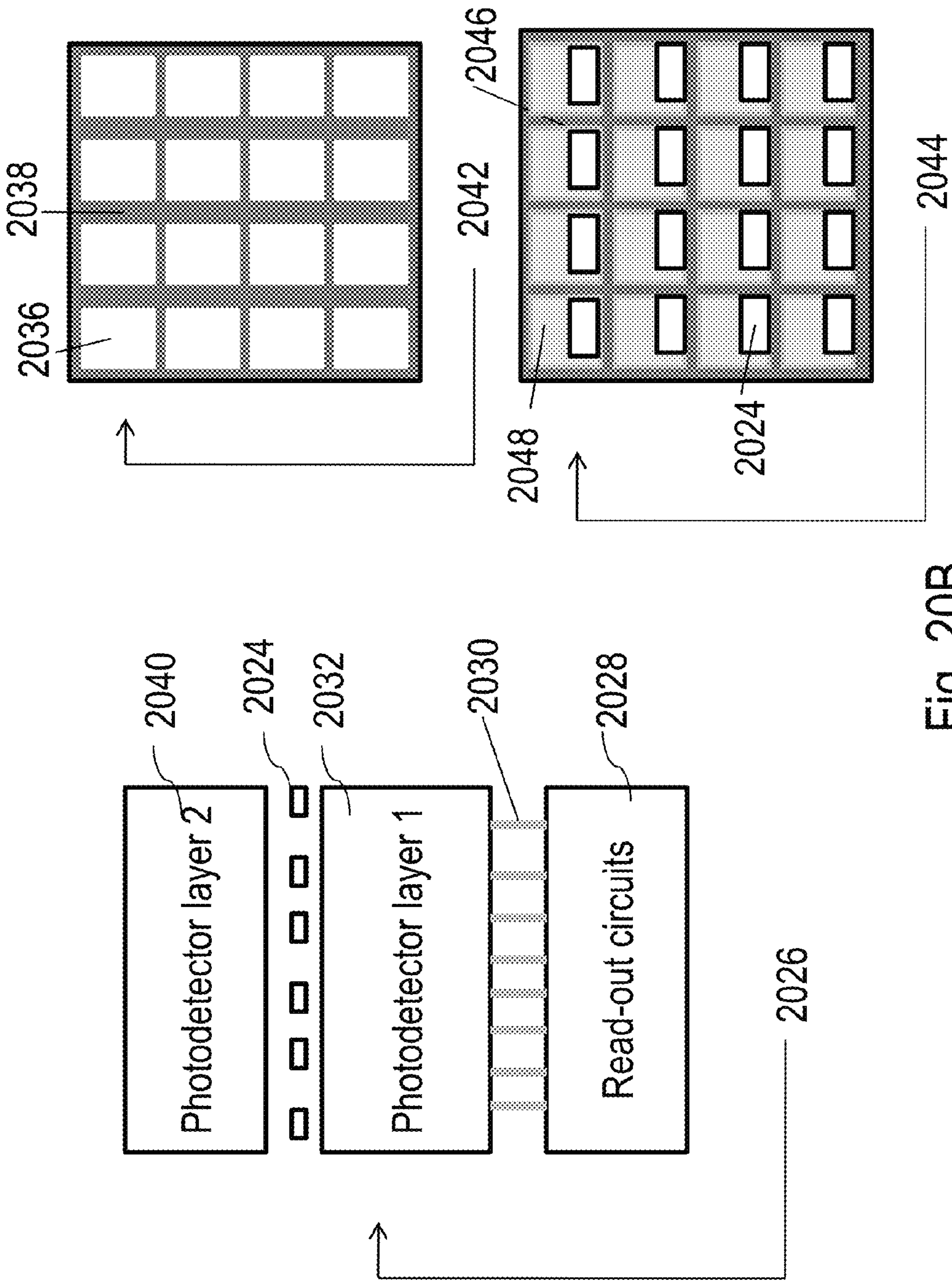

2036
2038
2042
2046
2048
2024
2044
2040
2024
2032
2030
2028
Photodetector layer 2
Photodetector layer 1
Read-out circuits
2026

Fig. 20B

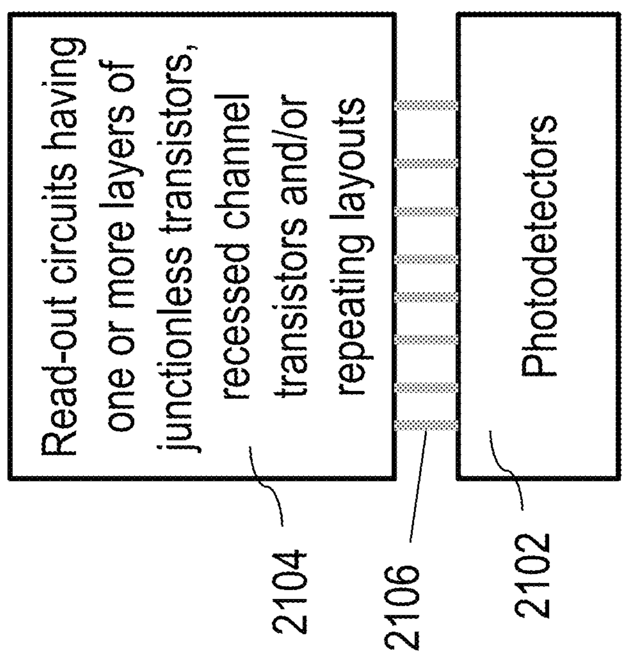

Read-out circuits having one or more layers of junctionless transistors, recessed channel transistors and/or repeating layouts
Photodetectors
2104
2106
2102

Fig. 21

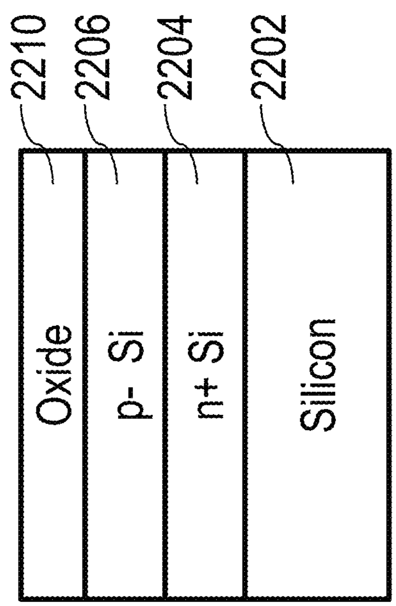
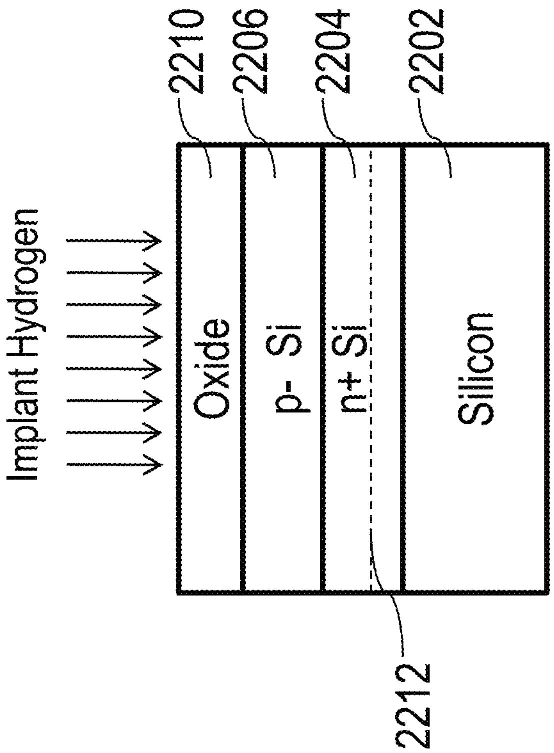


Fig. 22A



Implant Hydrogen
Oxide
p- Si
n+ Si
Silicon
2210
2206
2204
2202
2212

Fig. 22B

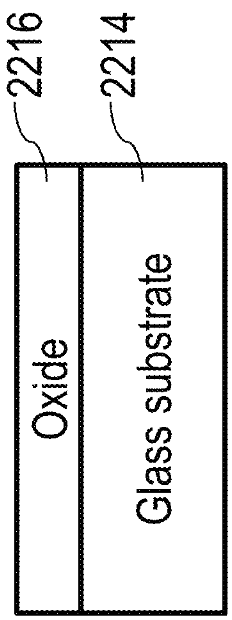


Fig. 22C

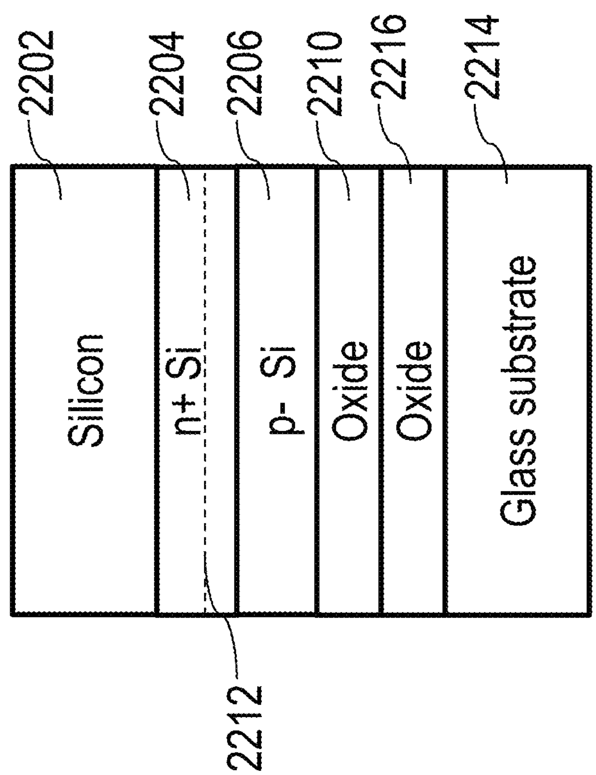

2202
2204
2206
2210
2216
2214
Silicon
n+ Si
p- Si
Oxide
Oxide
Glass substrate
2212

Fig. 22D

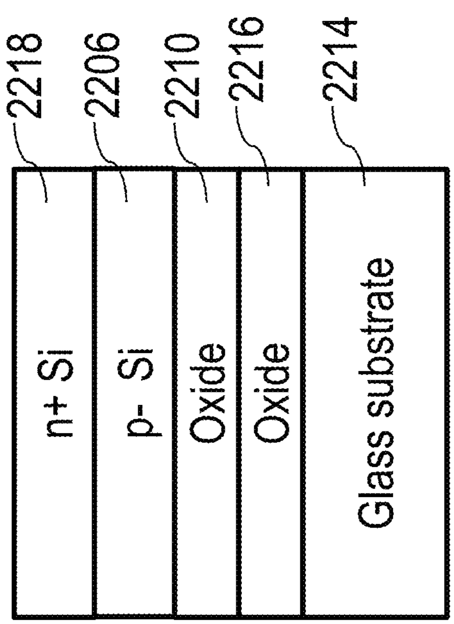

2218
2206
2210
2216
2214
n+ Si
p- Si
Oxide
Oxide
Glass substrate

Fig. 22E

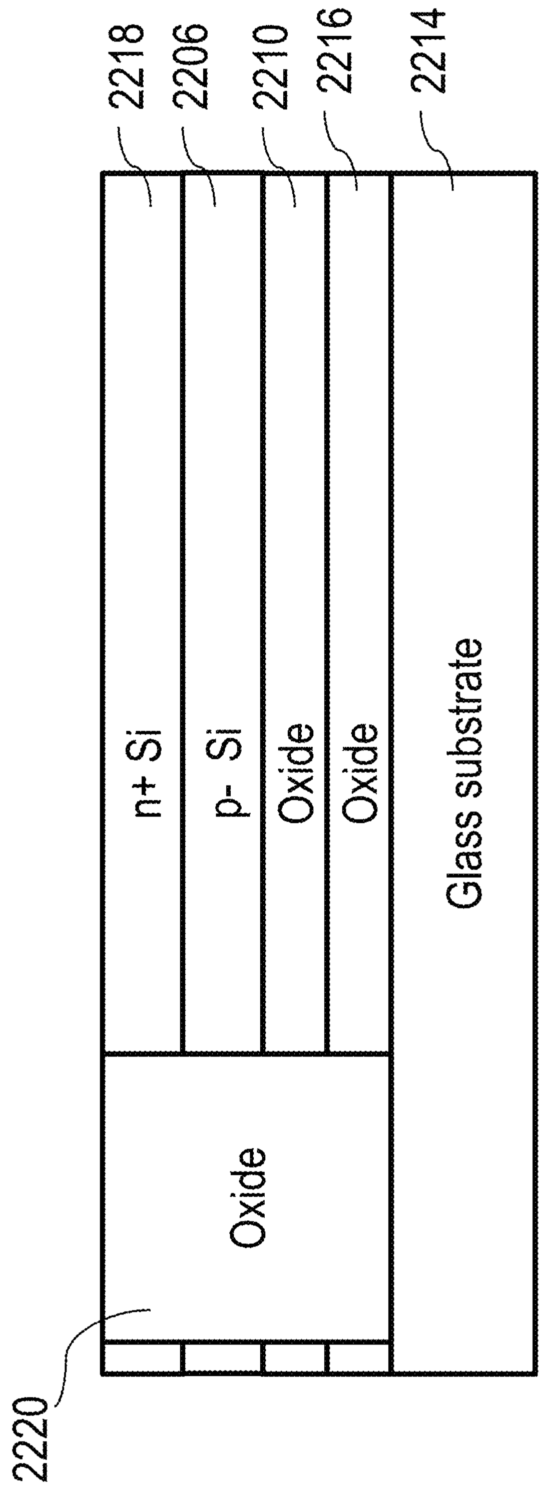

2218
2206
2210
2216
2214
n+ Si
p- Si
Oxide
Oxide
Glass substrate
Oxide
2220

Fig. 22F

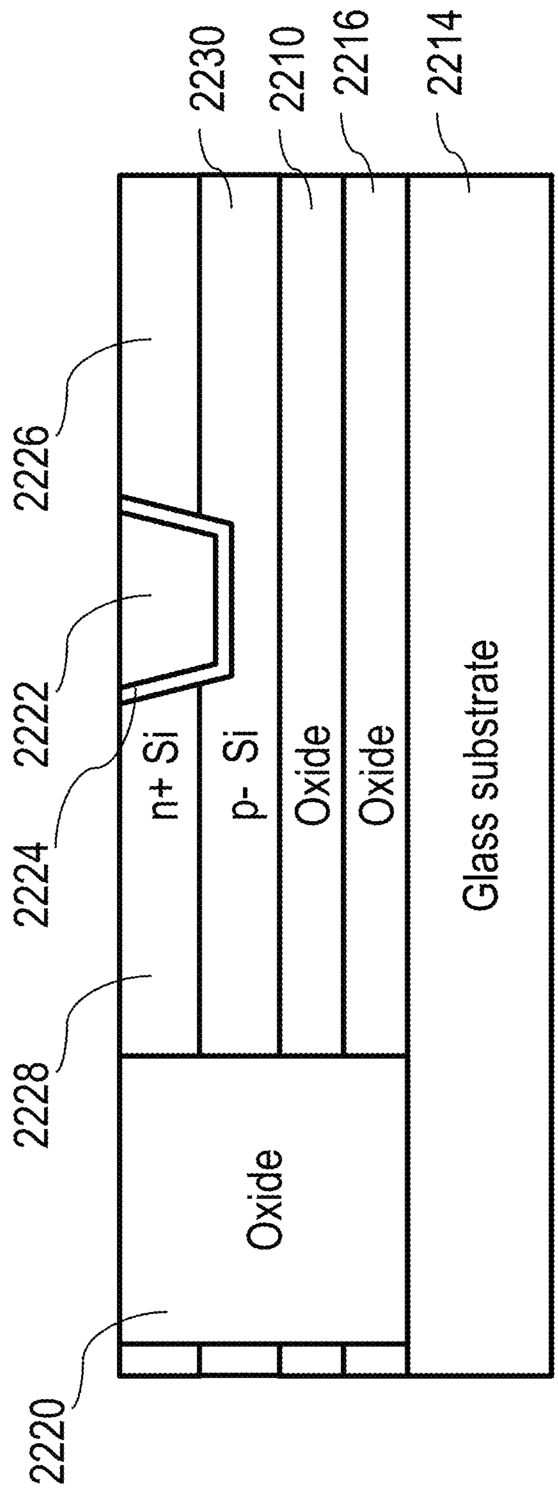

2230
2210
2216
2214
2226
2222
2224
2228
2220
n+ Si
p- Si
Oxide
Oxide
Glass substrate
Oxide

Fig. 22G

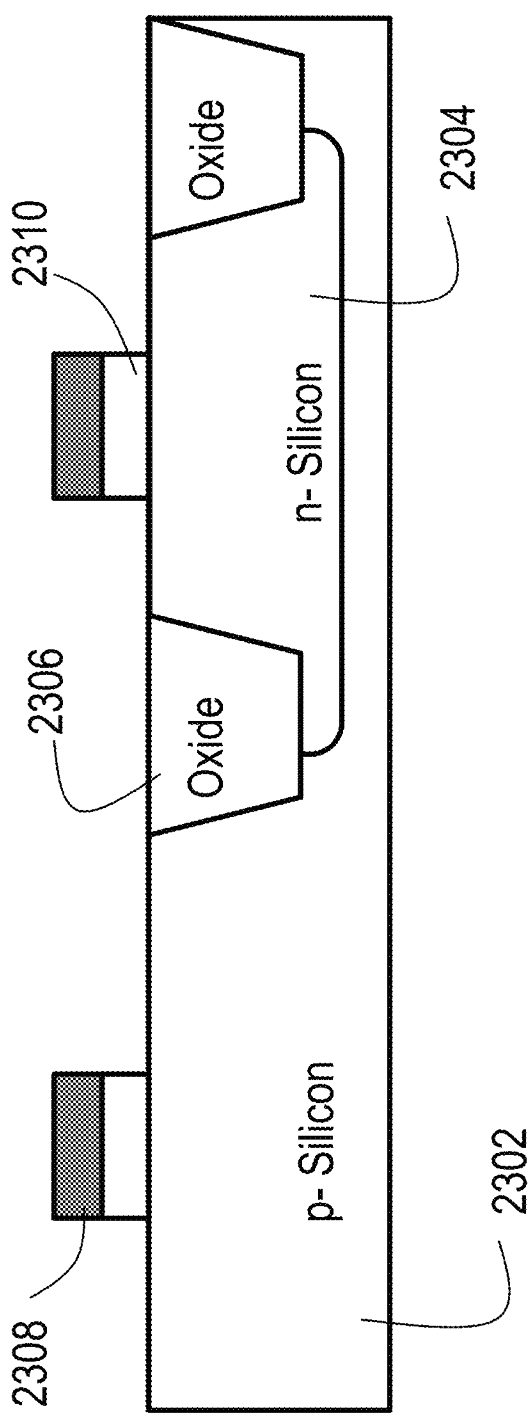
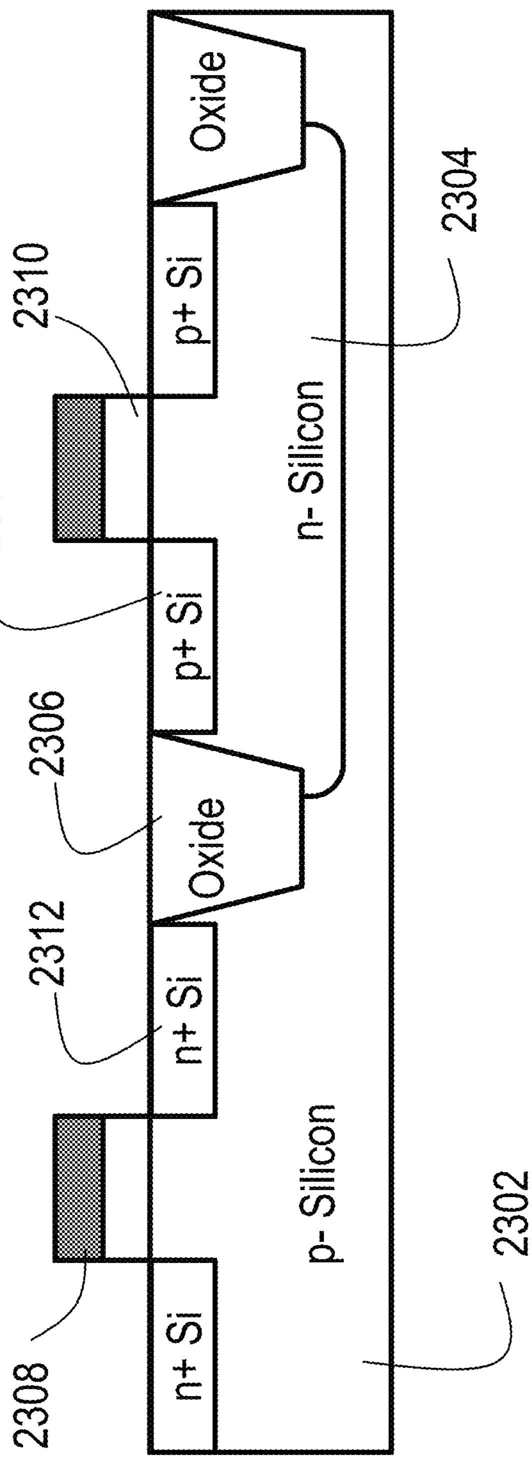


Fig. 23A



Oxide
2304
p+ Si
2310
n- Silicon
2314
p+ Si
2306
Oxide
2312
n+ Si
p- Silicon
2302
n+ Si
2308

Fig. 23B

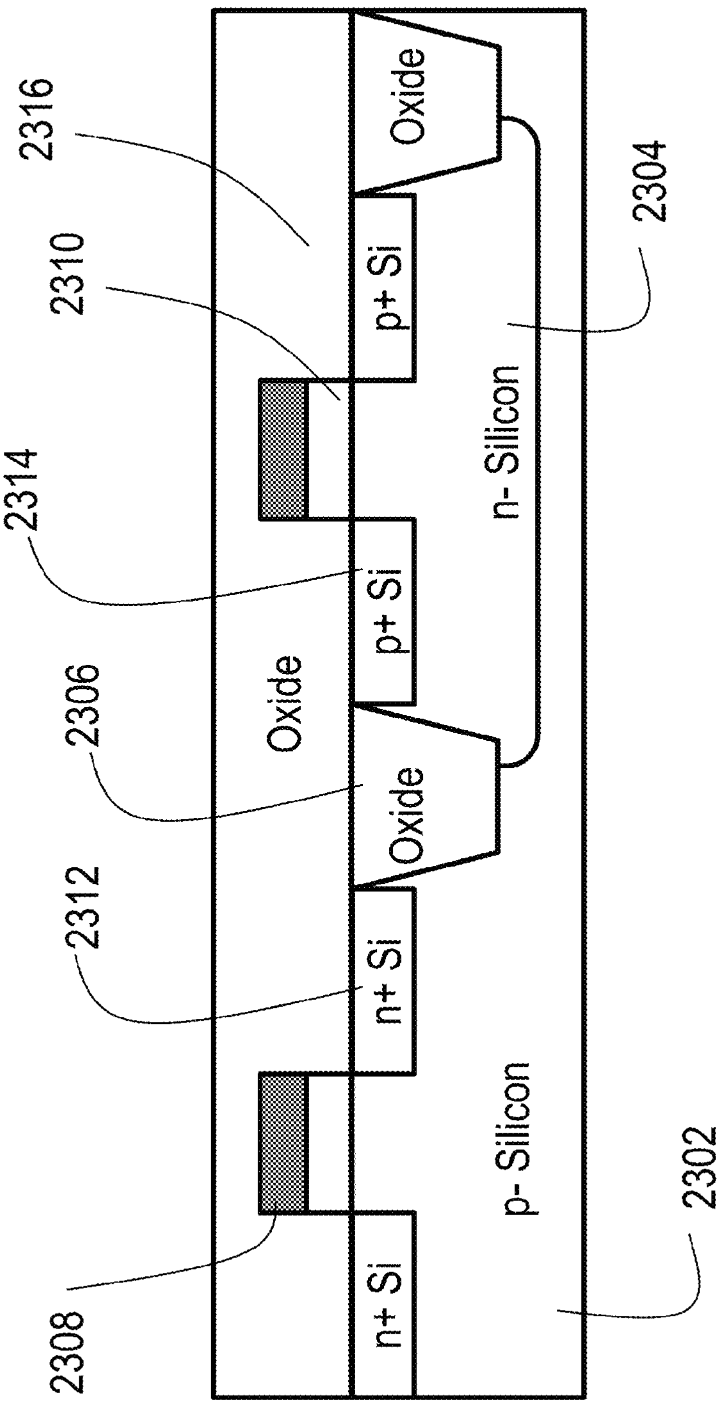

2316
2310
2314
2306
2312
2308
Oxide
Oxide
p+ Si
p+ Si
Oxide
n+ Si
n+ Si
n- Silicon
p- Silicon
2304
2302

Fig. 23C

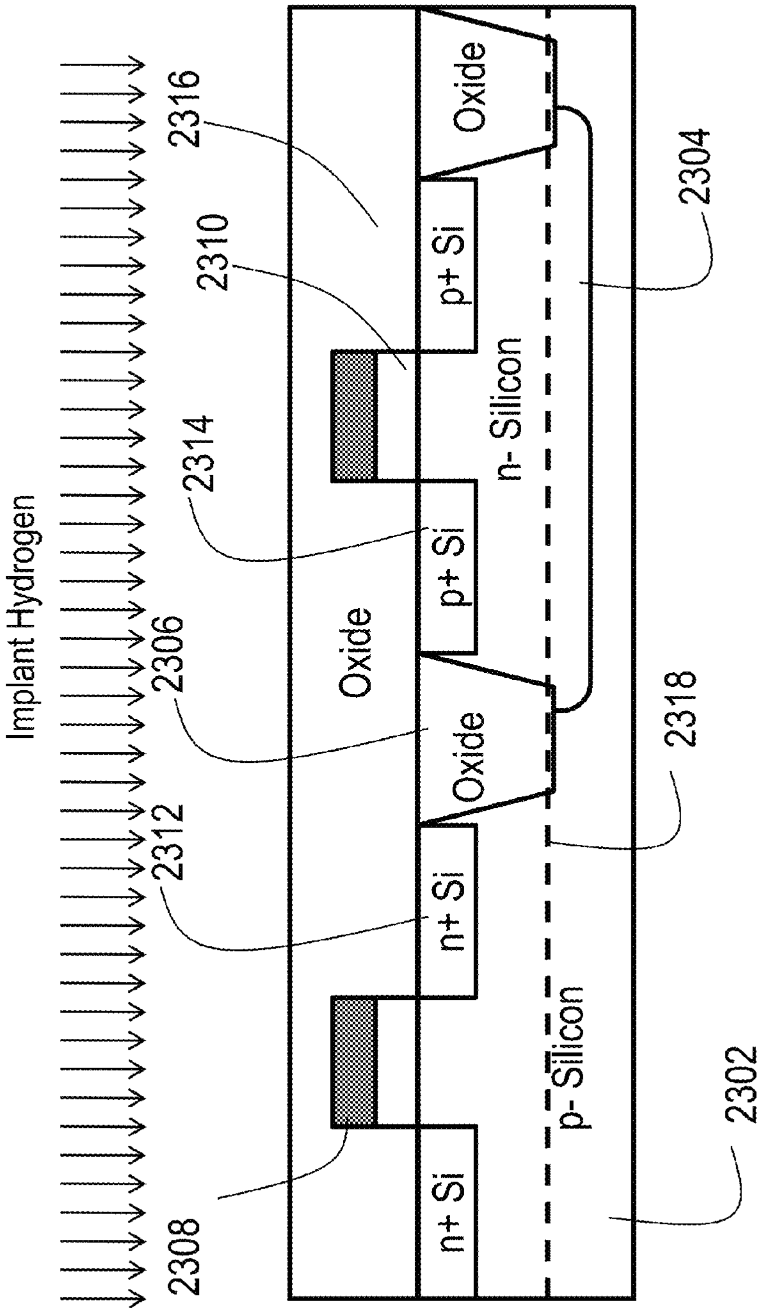
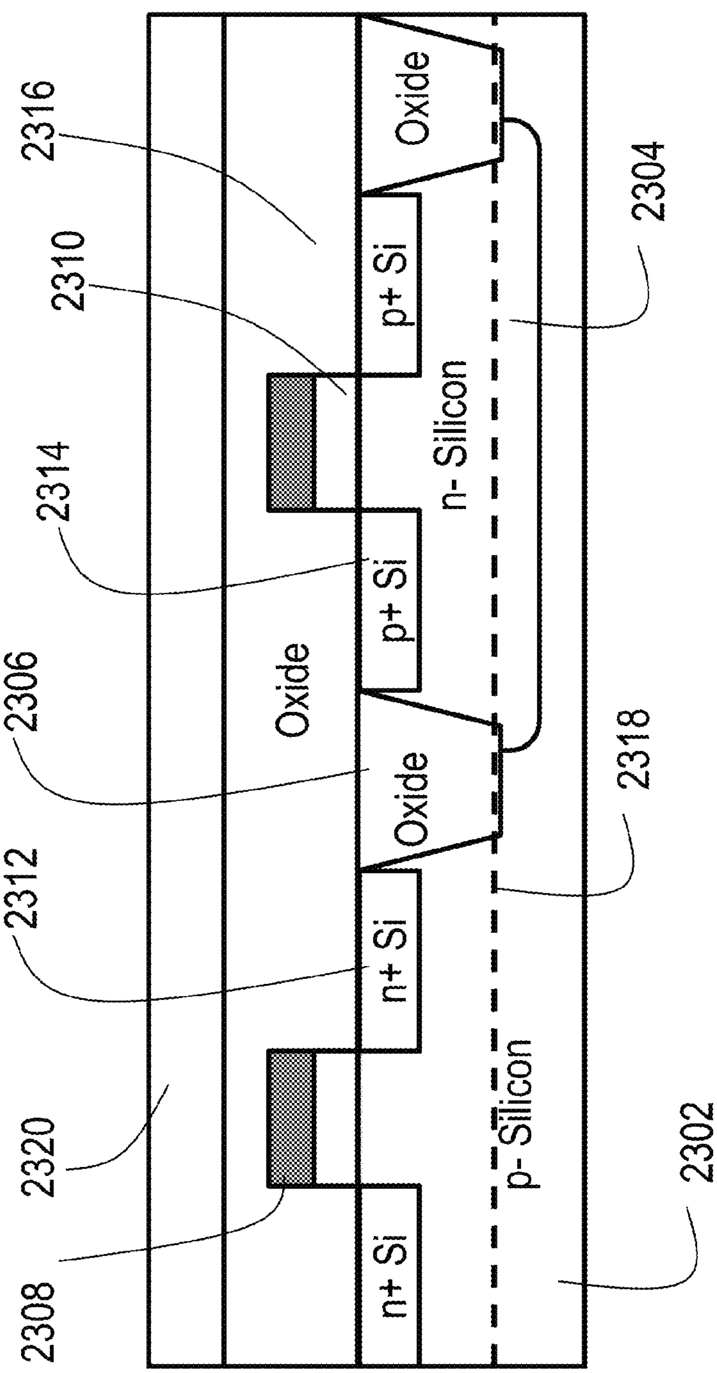

Implant Hydrogen
2316
2310
2314
2306
2312
2308
Oxide
Oxide
p+ Si
p+ Si
Oxide
n+ Si
n+ Si
n- Silicon
p- Silicon
2304
2318
2302

Fig. 23D



2316
2310
2314
2306
2312
2320
2308
Oxide
p+ Si
n- Silicon
p+ Si
Oxide
Oxide
n+ Si
p- Silicon
n+ Si
2304
2318
2302

Fig. 23E

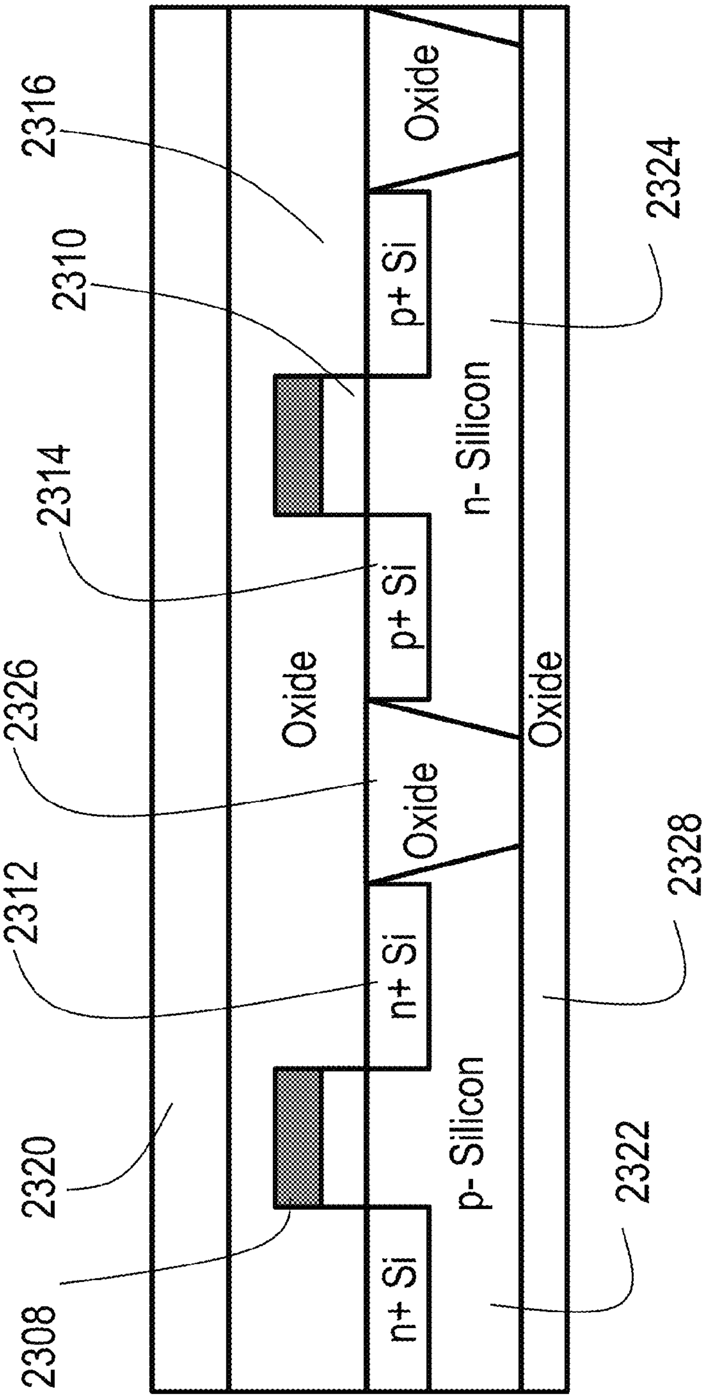

2316
2310
2314
2326
2312
2320
2308
2324
2328
2322
Oxide
p+ Si
n- Silicon
p+ Si
Oxide
Oxide
Oxide
n+ Si
p- Silicon
n+ Si

Fig. 23F

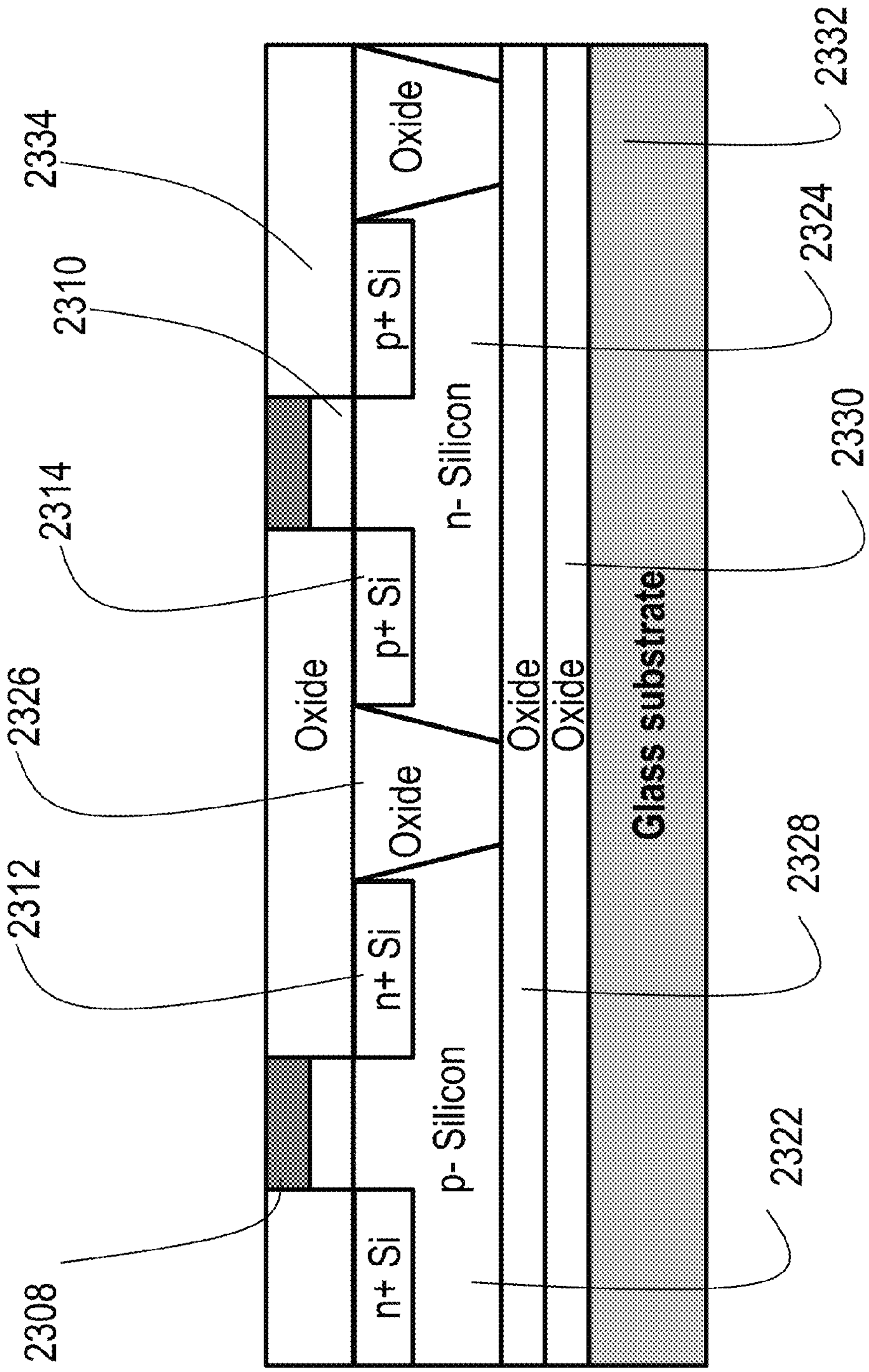

2334
2310
2314
2326
2312
2308
Oxide
p+ Si
n- Silicon
p+ Si
Oxide
Oxide
Oxide
Oxide
n+ Si
p- Silicon
n+ Si
Glass substrate
2332
2324
2330
2328
2322

Fig. 23G

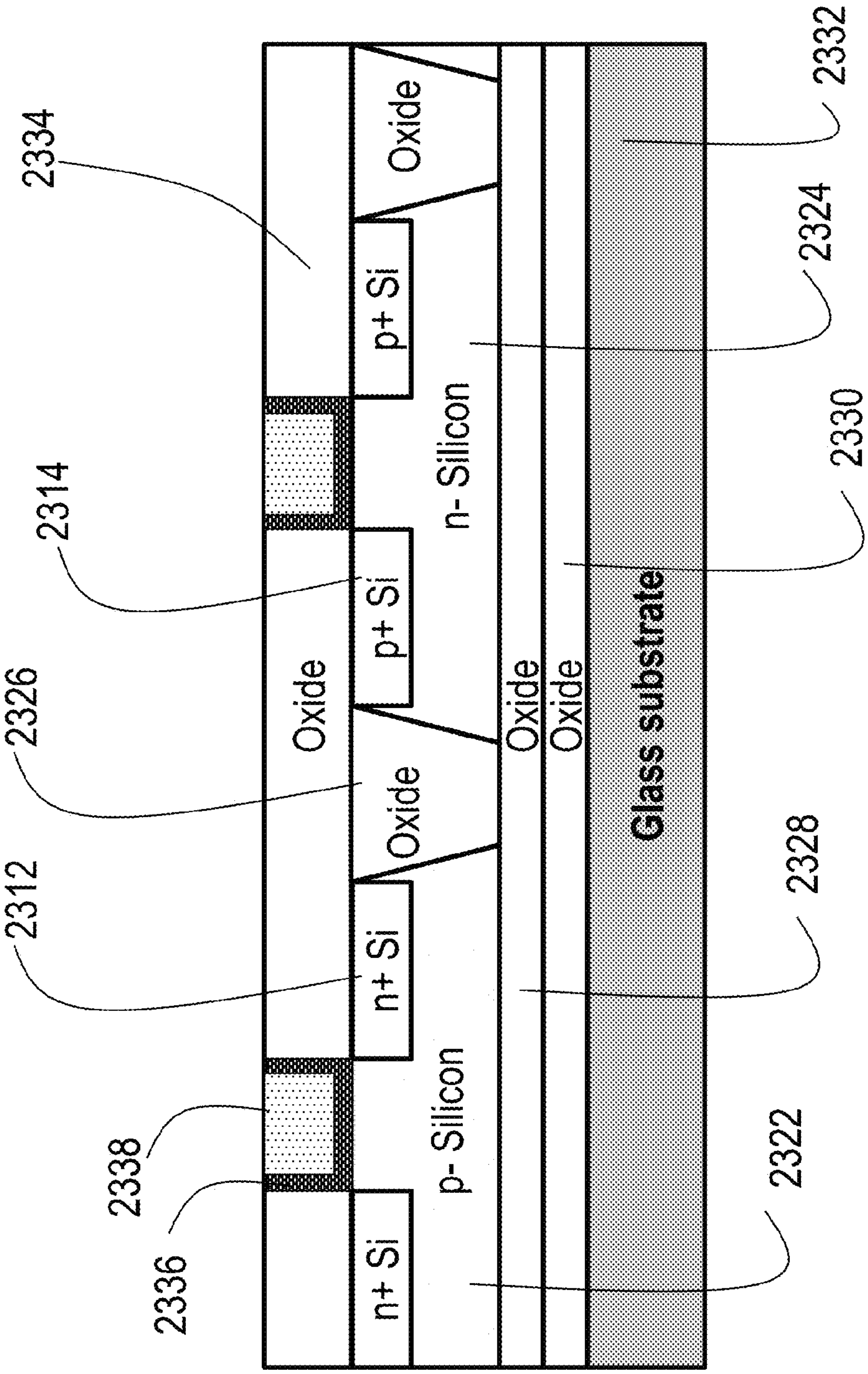

2334
2314
2326
2312
2338
2336
2332
2324
2330
2328
2322
Oxide
p+ Si
n- Silicon
p+ Si
Oxide
Oxide
Oxide
Oxide
n+ Si
p- Silicon
n+ Si
Glass substrate

Fig. 23H

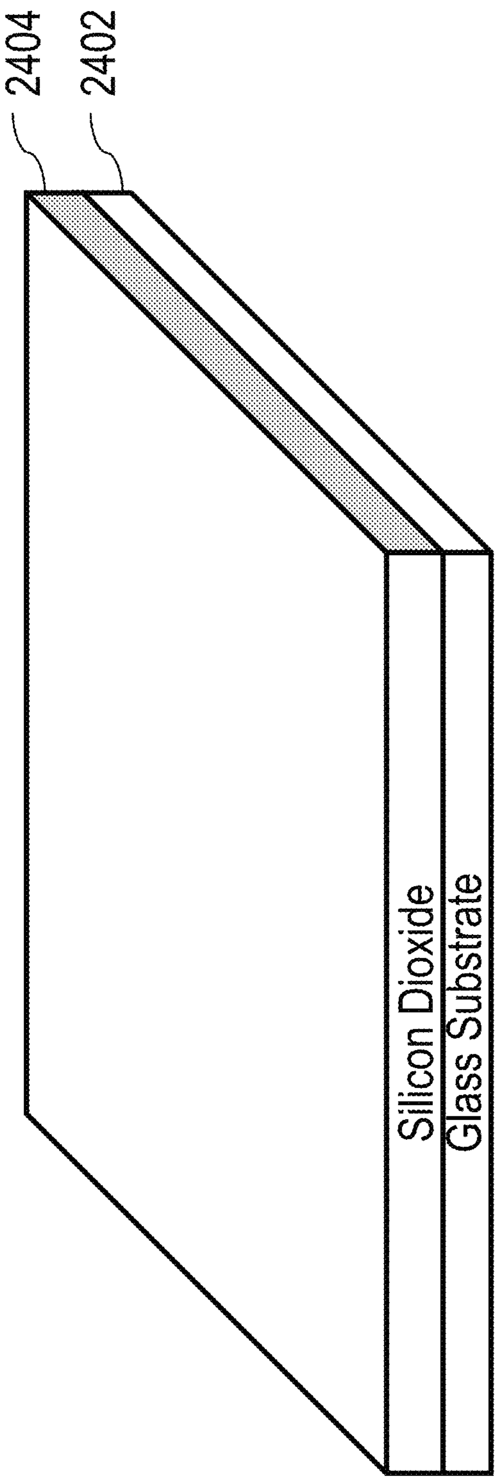


Fig. 24A

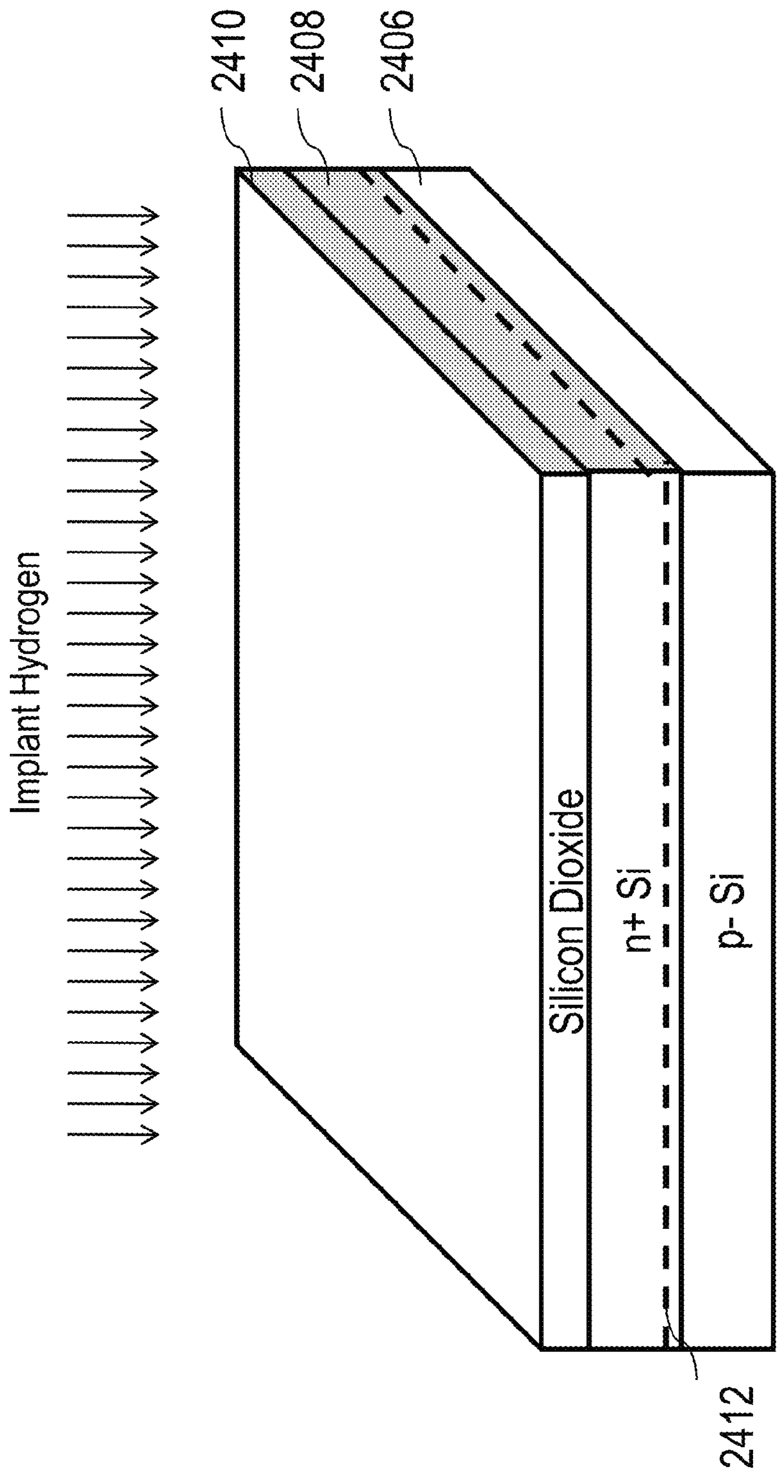

Implant Hydrogen
2410
2408
2406
Silicon Dioxide
n+ Si
p- Si
2412

Fig. 24B

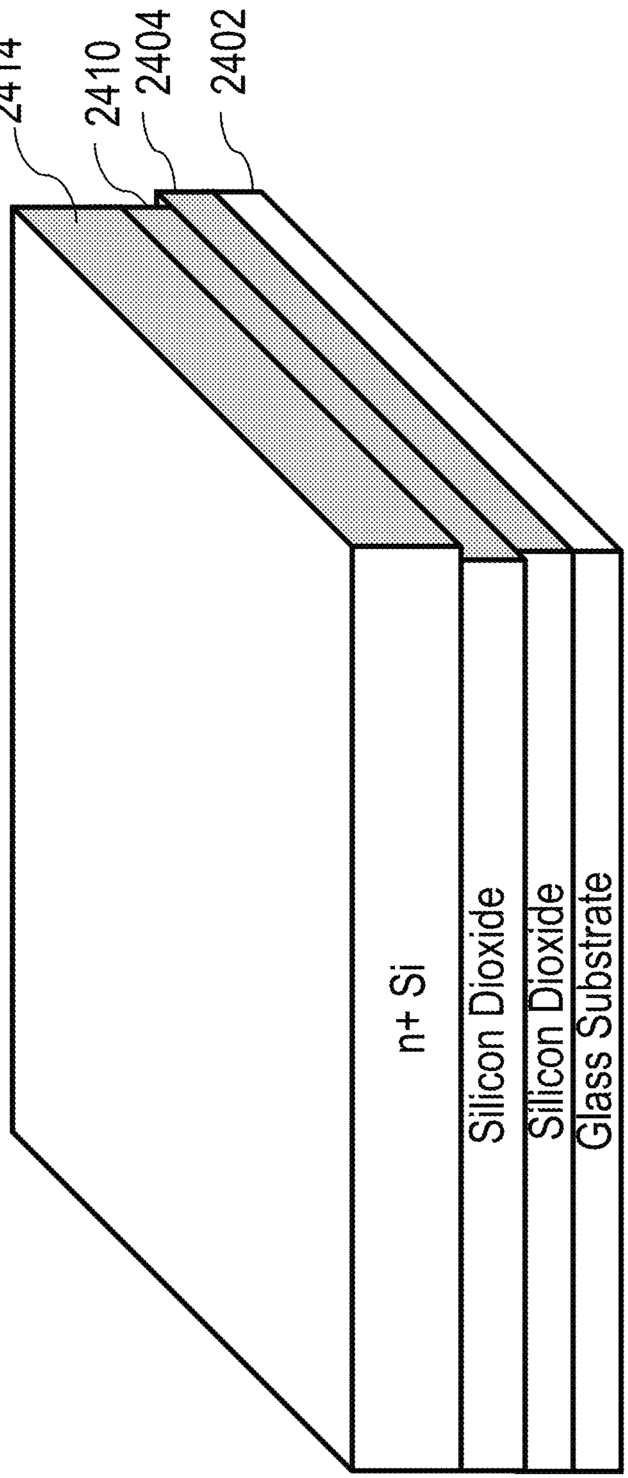

2414
2410
2404
2402
n+ Si
Silicon Dioxide
Silicon Dioxide
Glass Substrate

Fig. 24C

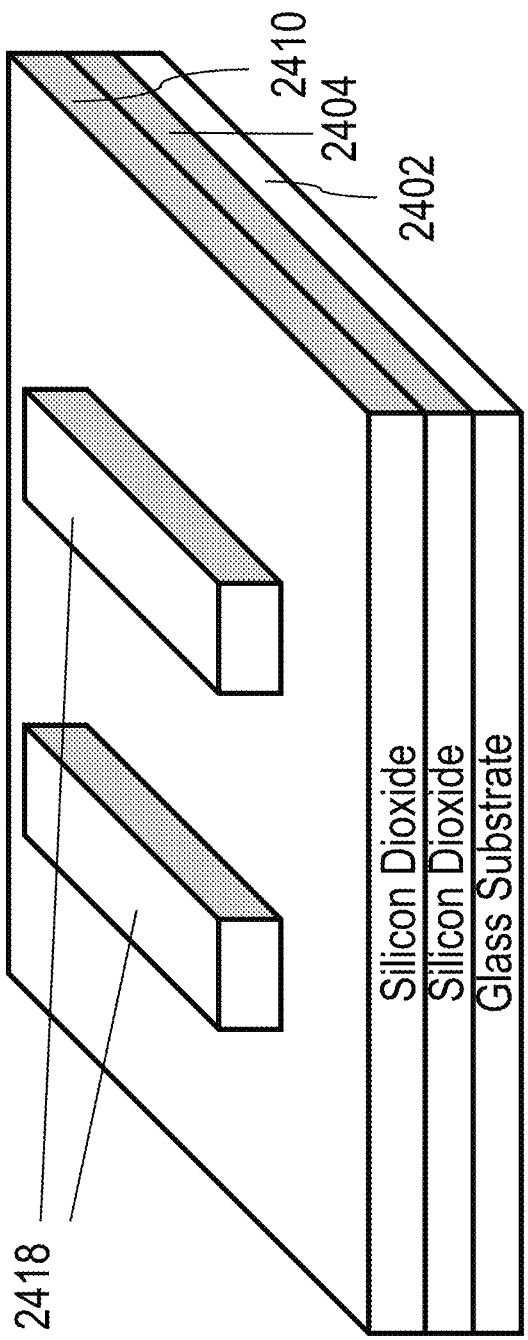
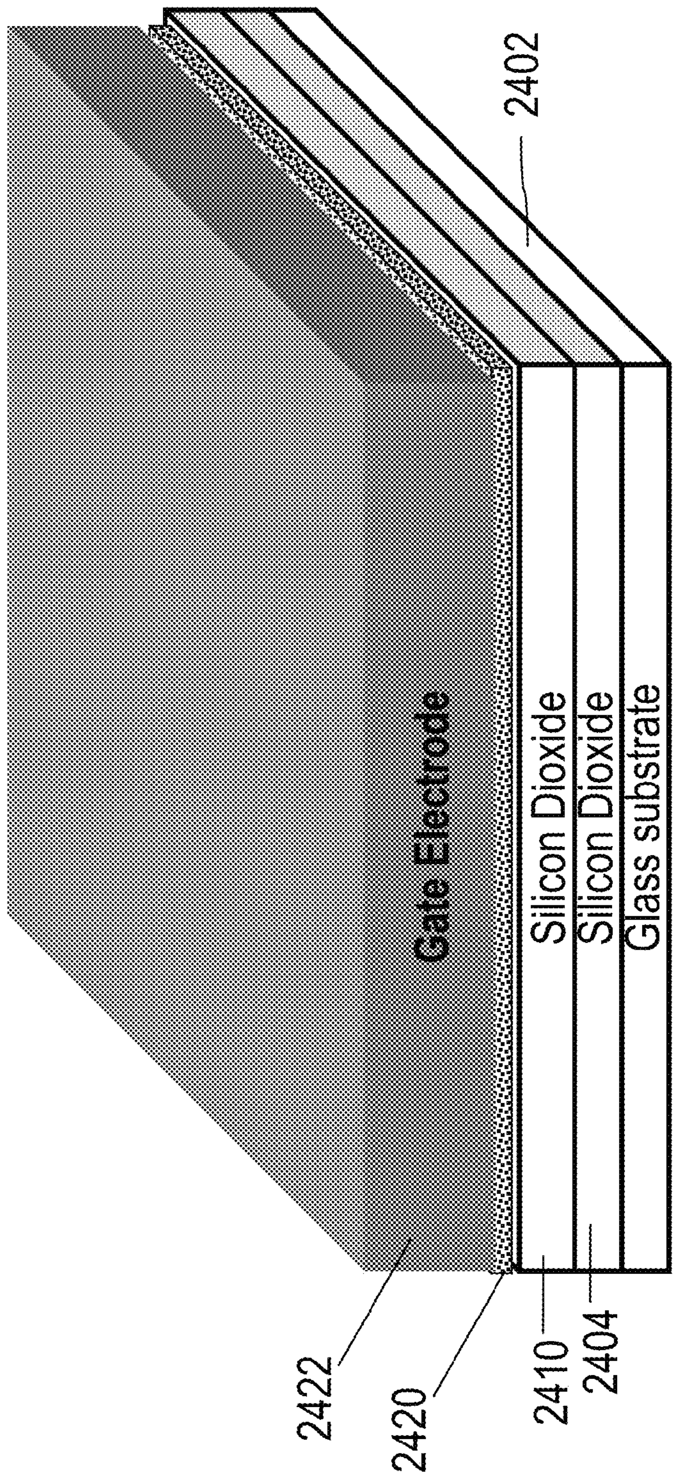

2410
2404
2402
Silicon Dioxide
Silicon Dioxide
Glass Substrate
2418

Fig. 24D



2402
Gate Electrode
Silicon Dioxide
Silicon Dioxide
Glass substrate
2422
2420
2410
2404

Fig. 24E

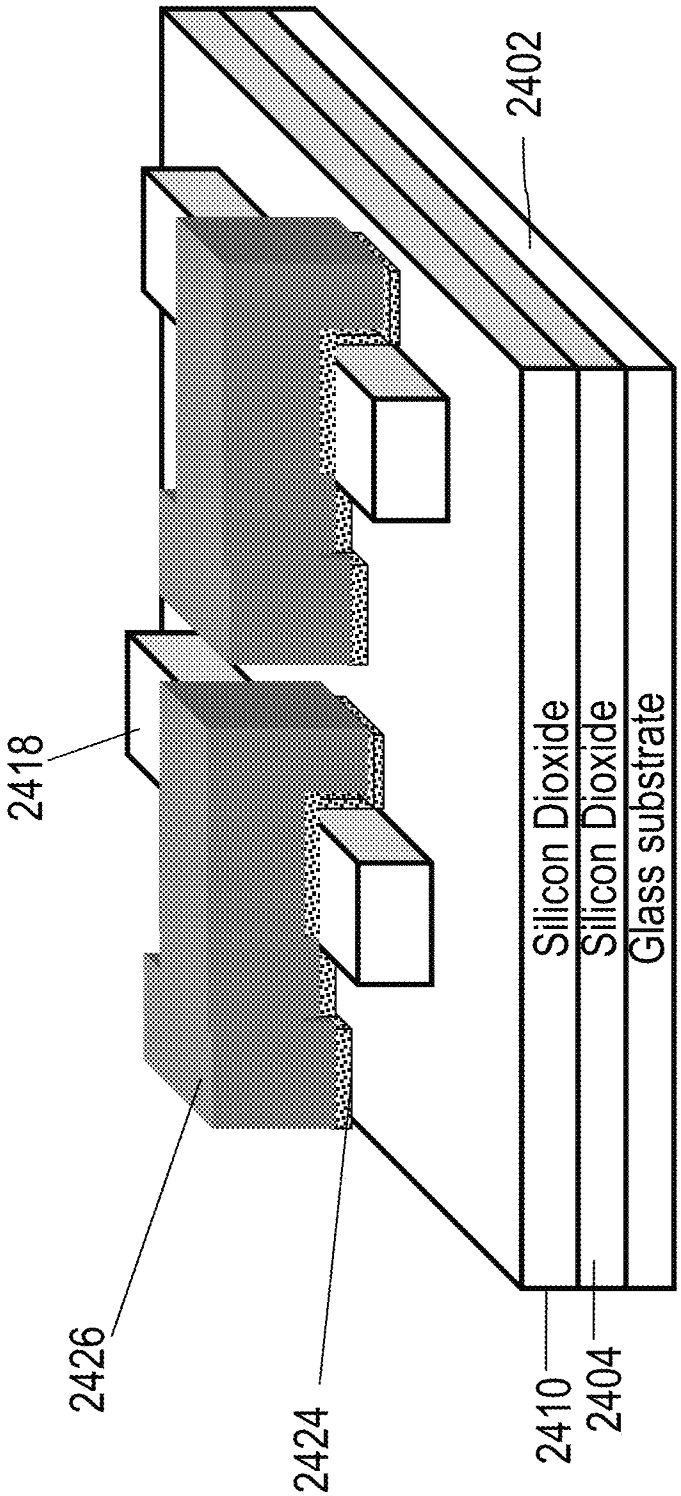

2402
2418
Silicon Dioxide
Silicon Dioxide
Glass substrate
2426
2424
2410
2404

Fig. 24F

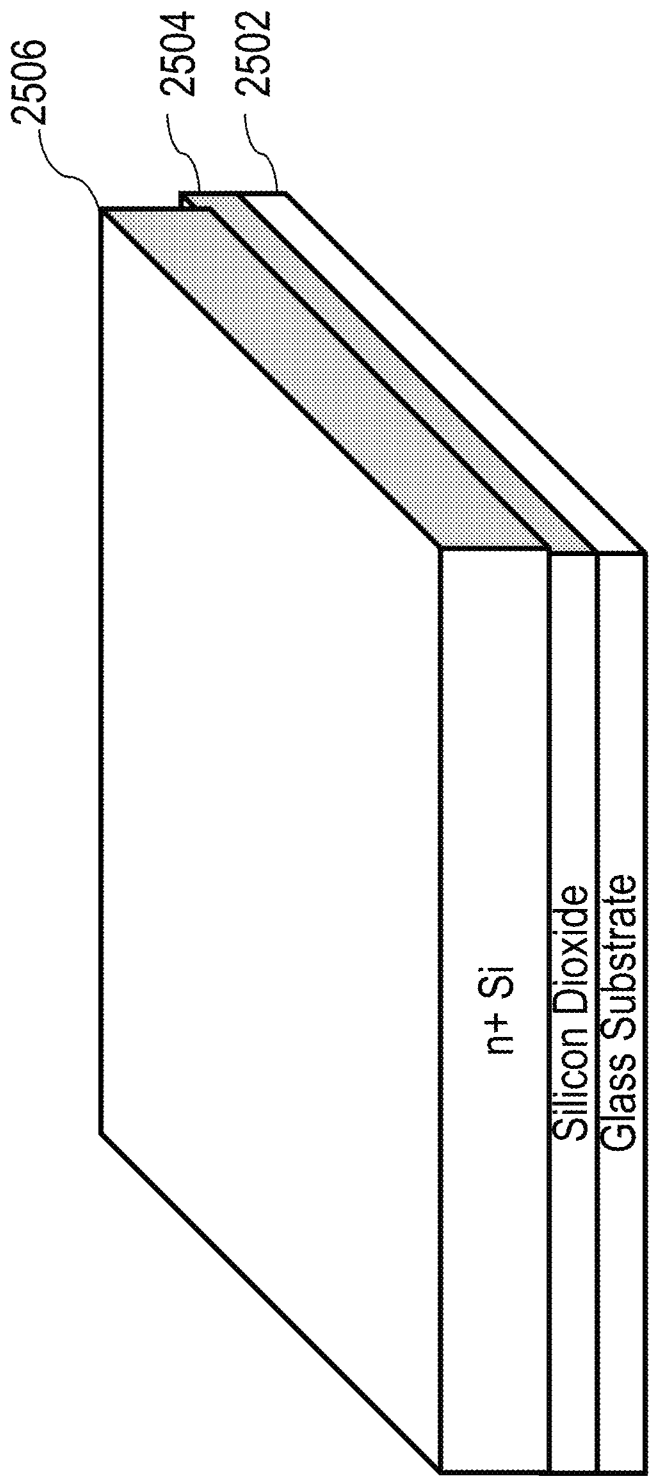


Fig. 25A

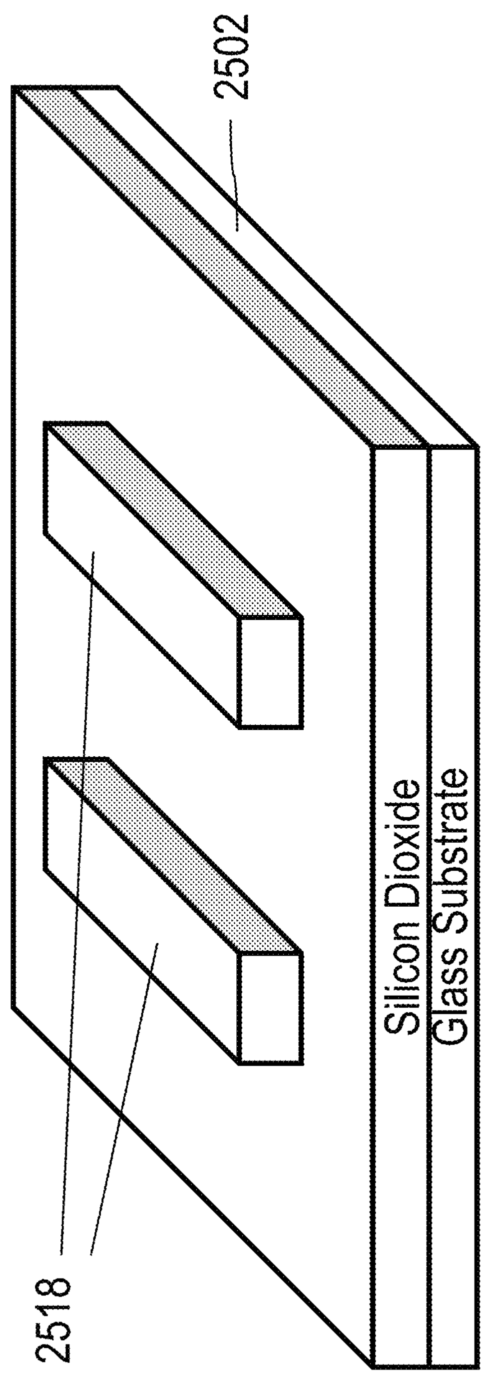


Fig. 25B

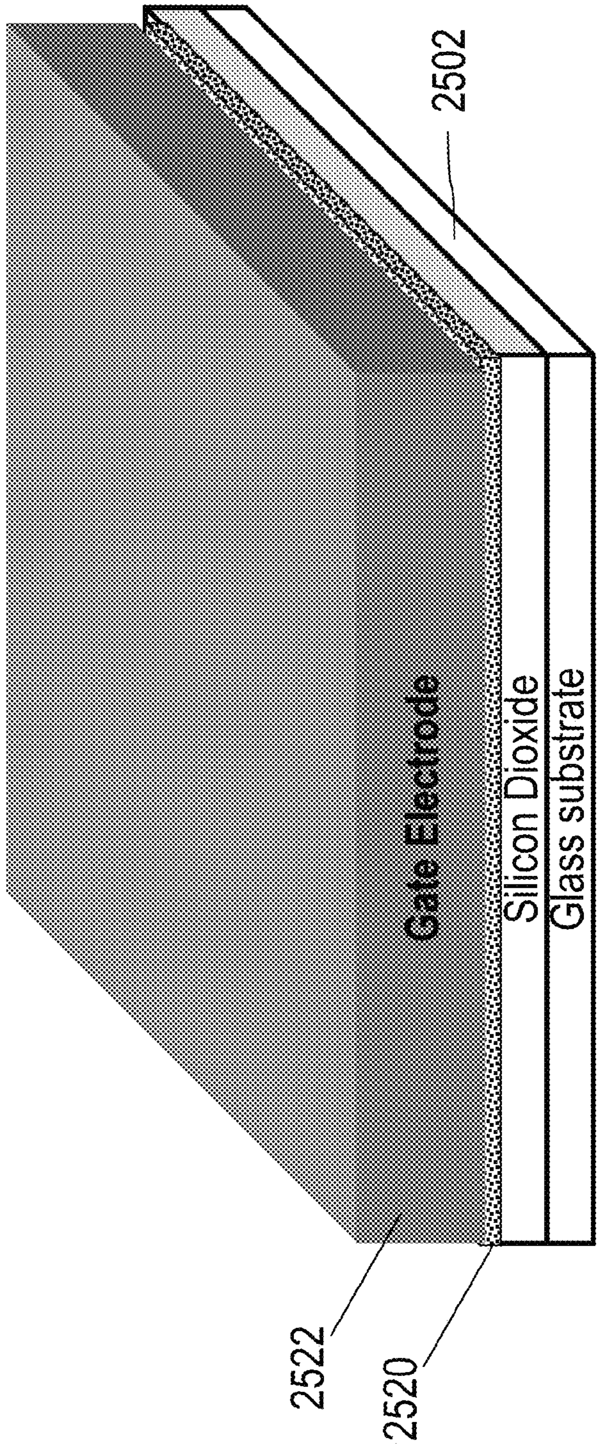

2502
Gate Electrode
Silicon Dioxide
Glass substrate
2522
2520

Fig. 25C

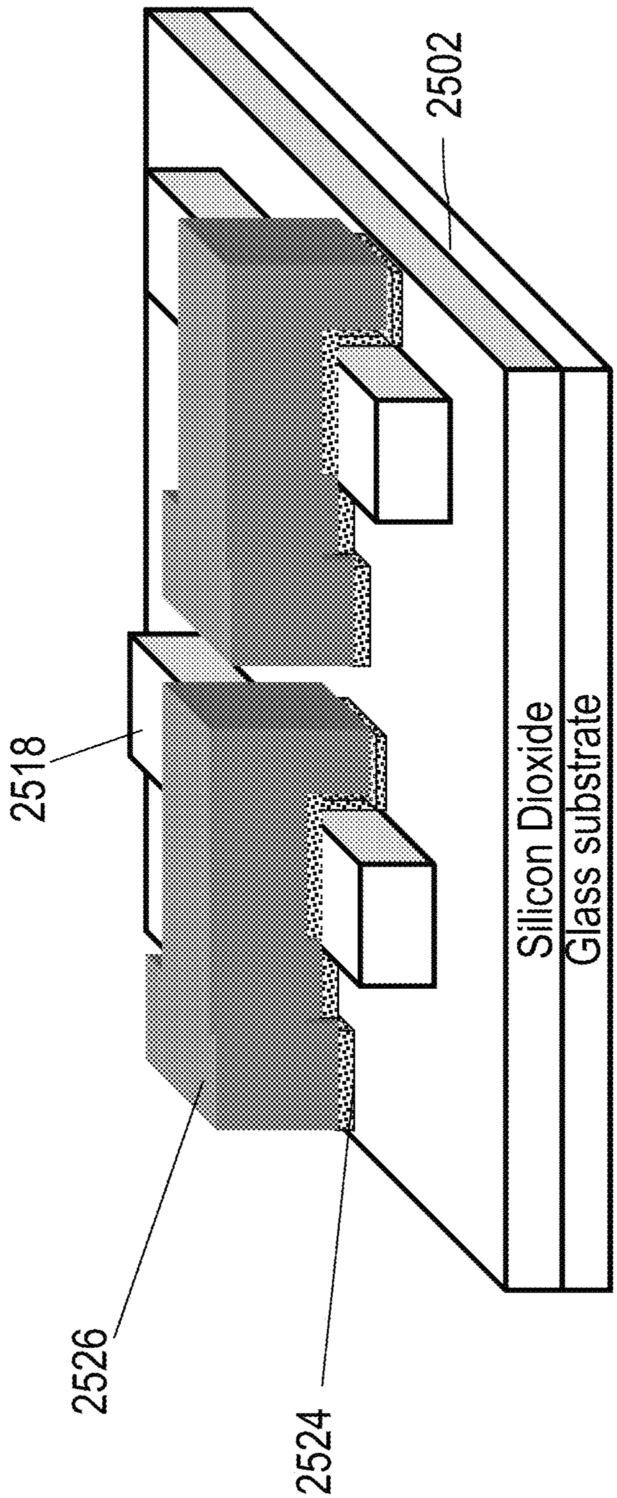
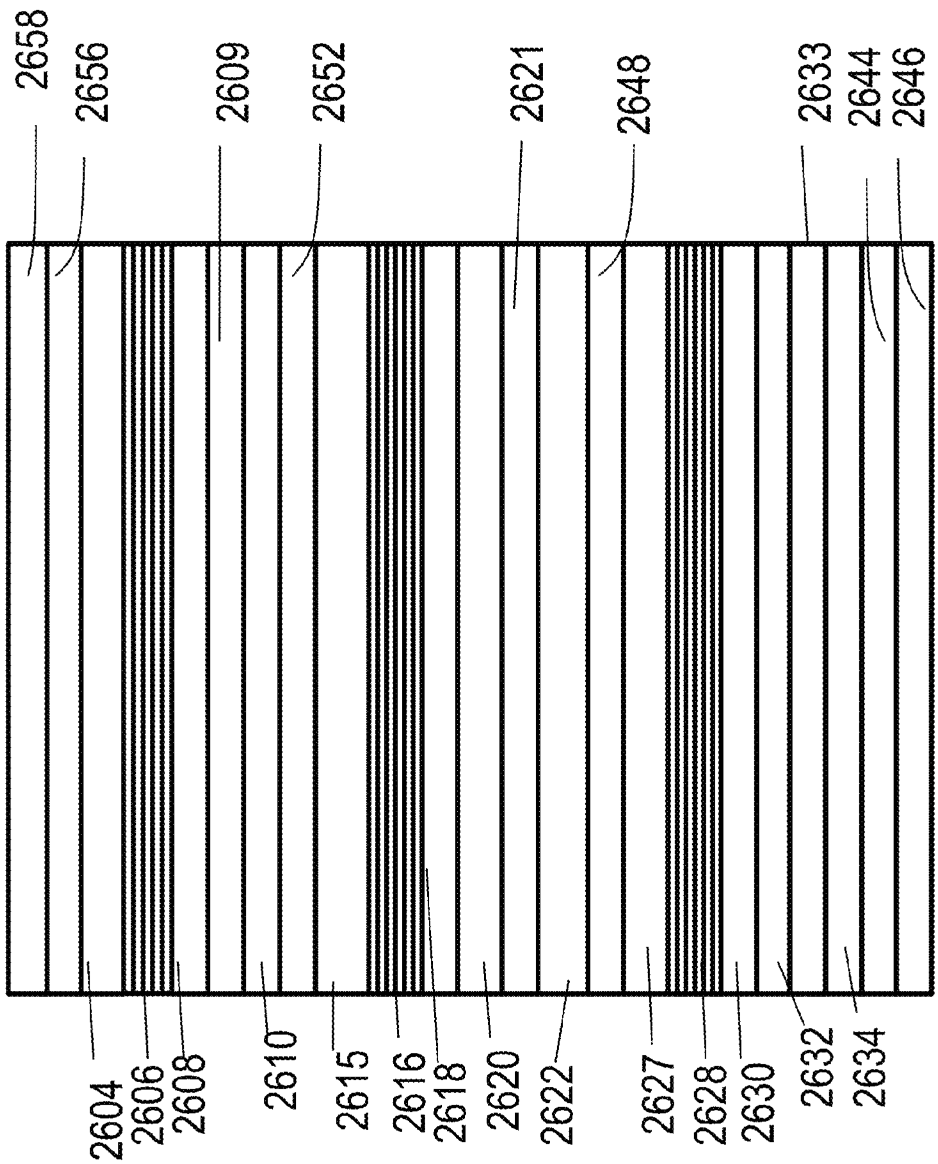


Fig. 25D

Fig. 26A


2658
2656
2609
2652
2621
2648
2633
2644
2646
2604
2606
2608
2610
2615
2616
2618
2620
2622
2627
2628
2630
2632
2634

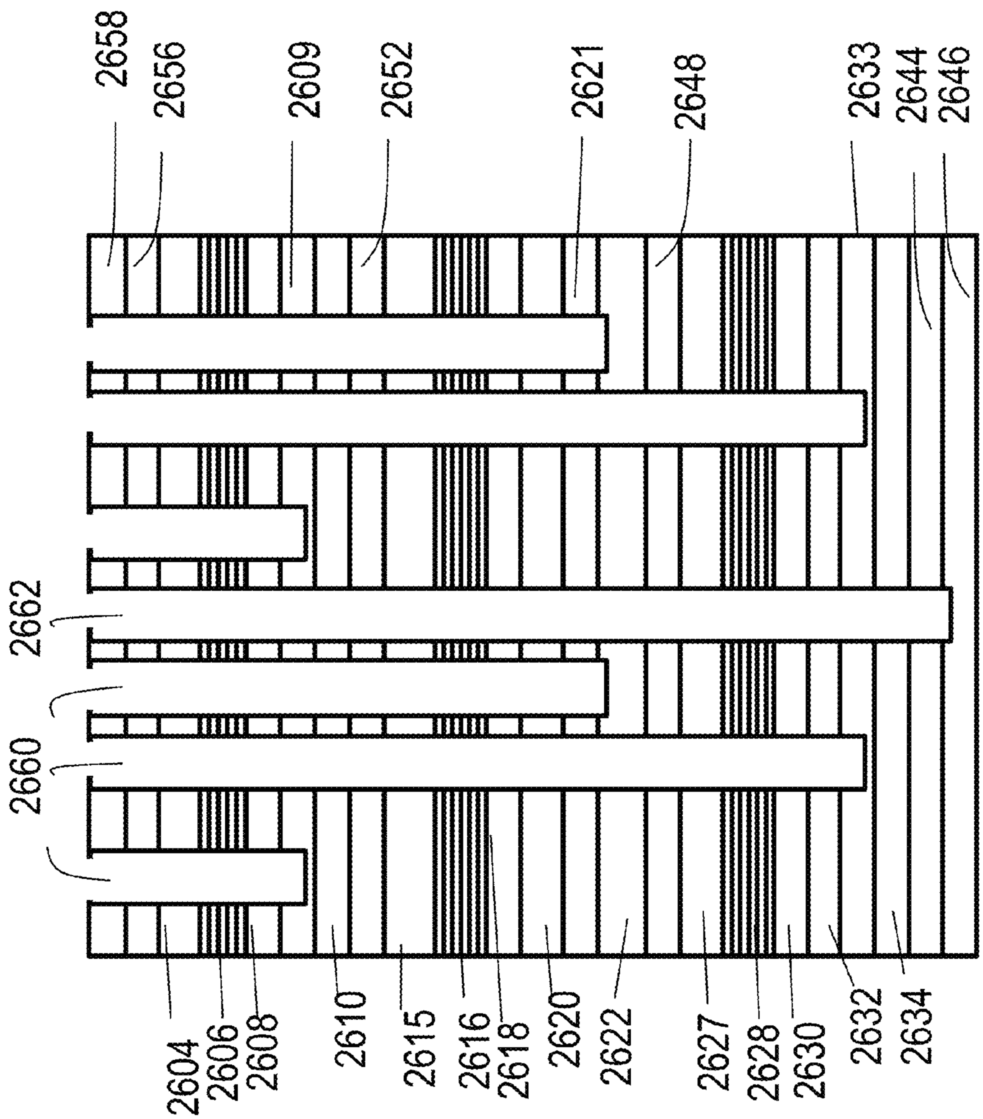
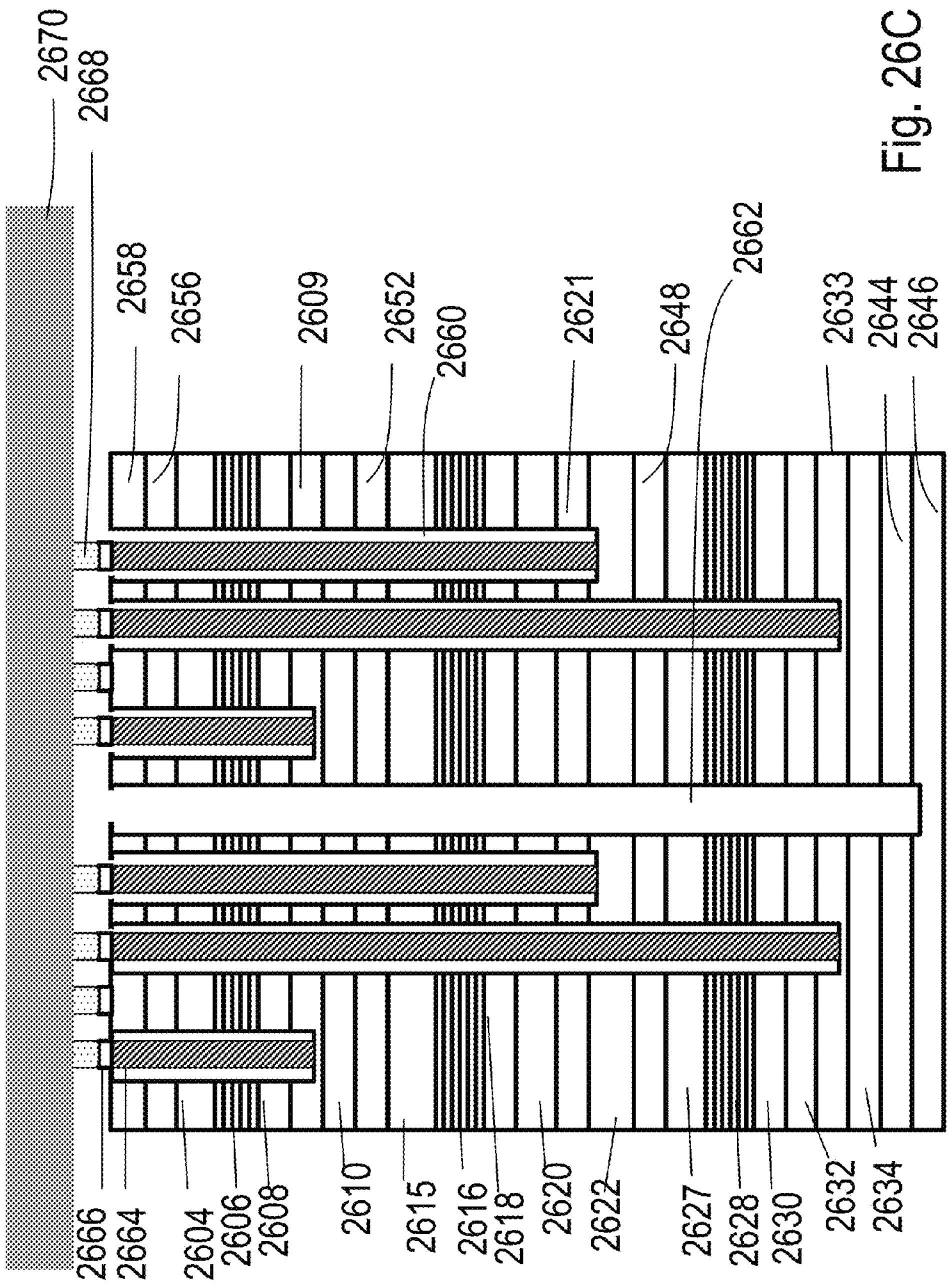

2658
2656
2609
2652
2621
2648
2633
2644
2646
2660
2662
2604
2606
2608
2610
2615
2616
2618
2620
2622
2627
2628
2630
2632
2634

Fig. 26B



2670
2668
2658
2656
2609
2652
2660
2621
2648
2662
2633
2644
2646
2666
2664
2604
2606
2608
2610
2615
2616
2618
2620
2622
2627
2628
2630
2632
2634

Fig. 26C

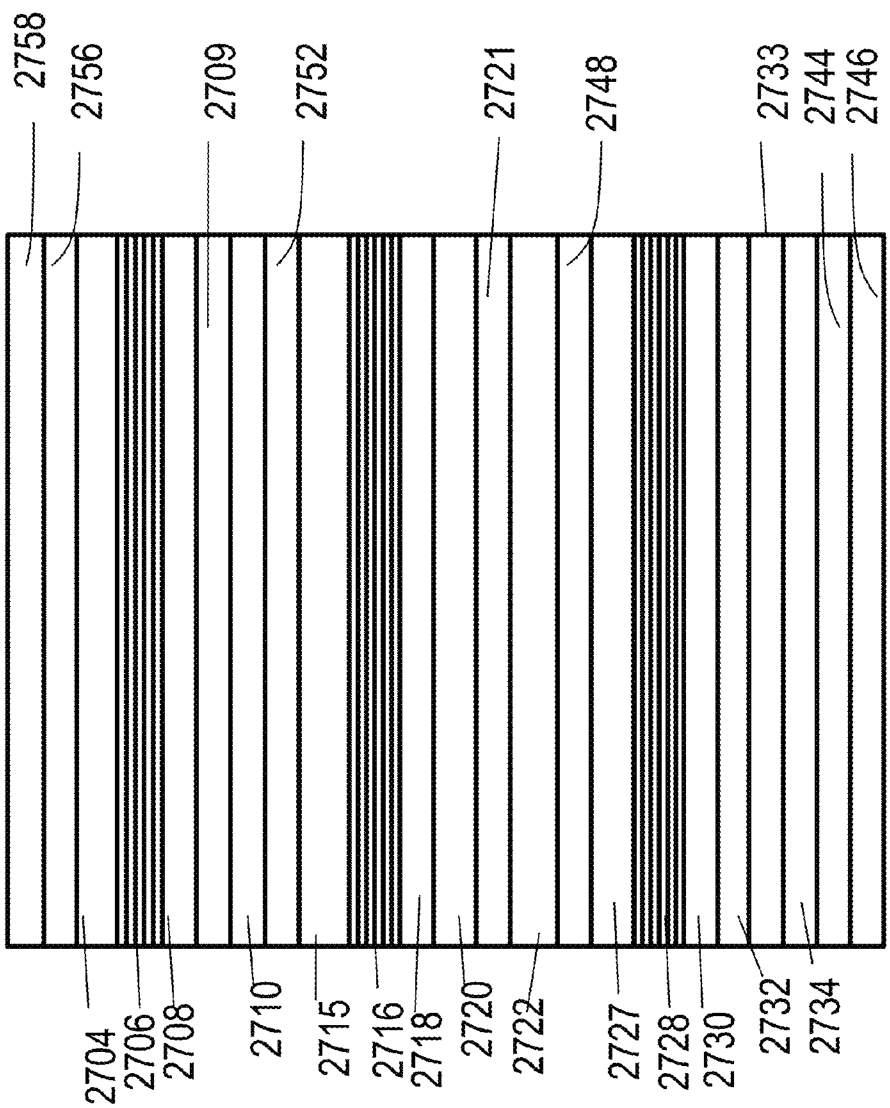

2758
2756
2709
2752
2721
2748
2733
2744
2746
2704
2706
2708
2710
2715
2716
2718
2720
2722
2727
2728
2730
2732
2734

Fig. 27A

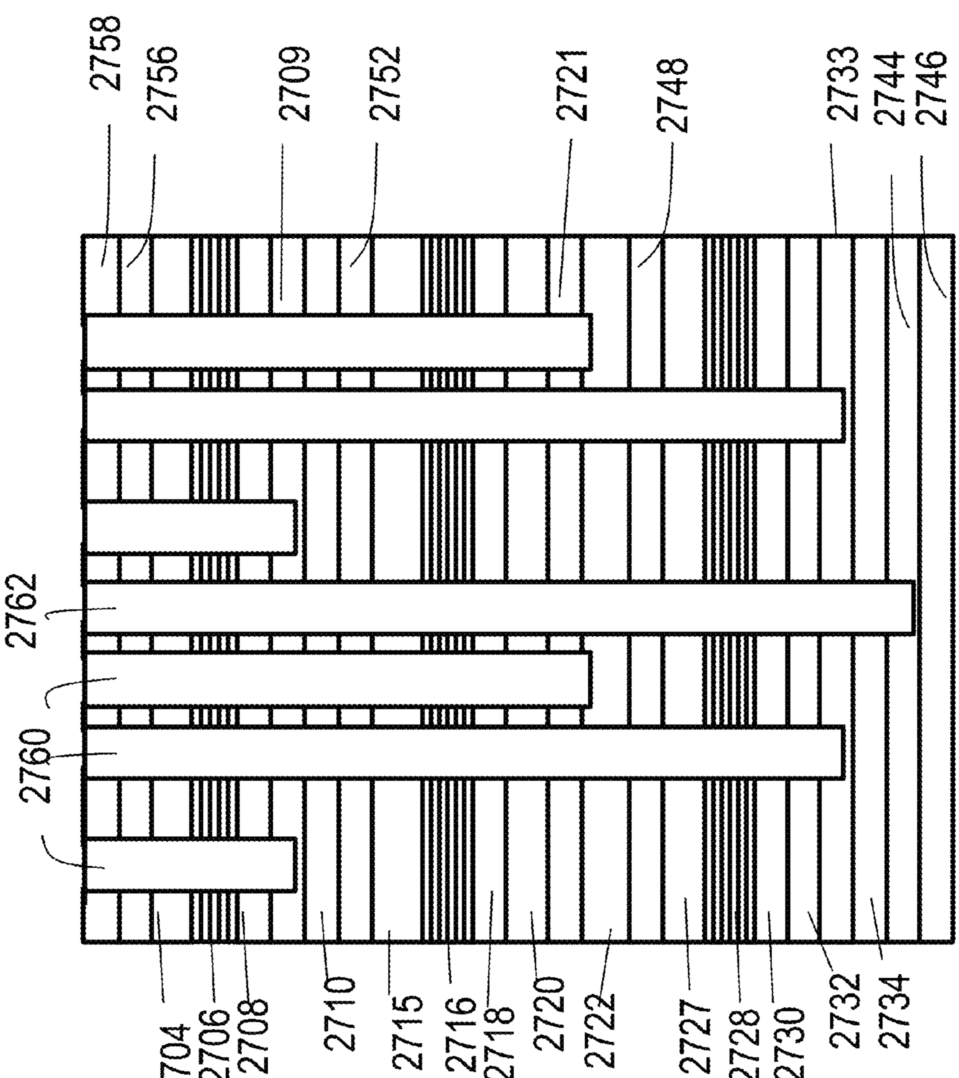

2758
2756
2709
2752
2721
2748
2733
2744
2746
2762
2760
2704
2706
2708
2710
2715
2716
2718
2720
2722
2727
2728
2730
2732
2734

Fig. 27B

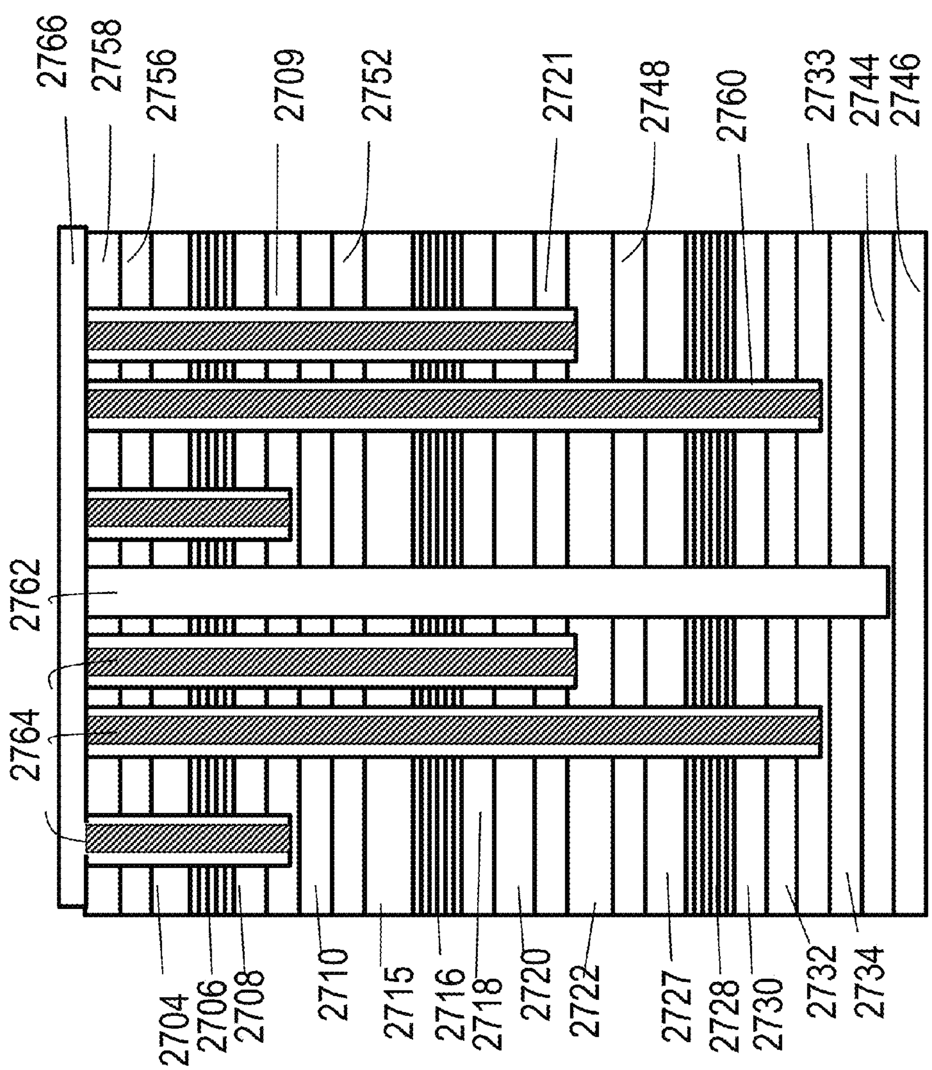

2766
2758
2756
2709
2752
2721
2748
2760
2733
2744
2746
2762
2764
2704
2706
2708
2710
2715
2716
2718
2720
2722
2727
2728
2730
2732
2734

Fig. 27C

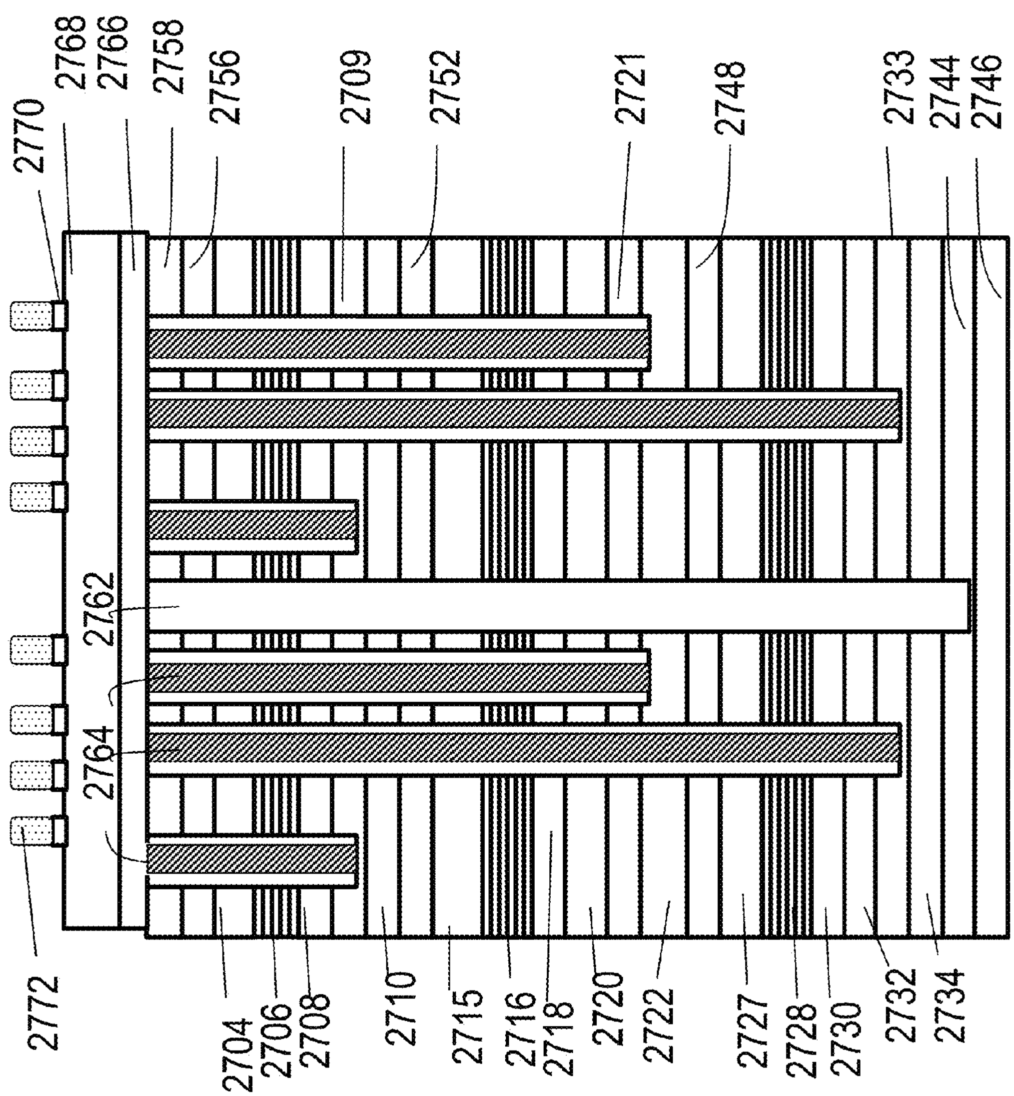

2770
2768
2766
2758
2756
2709
2752
2721
2748
2733
2744
2746
2762
2764
2772
2704
2706
2708
2710
2715
2716
2718
2720
2722
2727
2728
2730
2732
2734

Fig. 27D

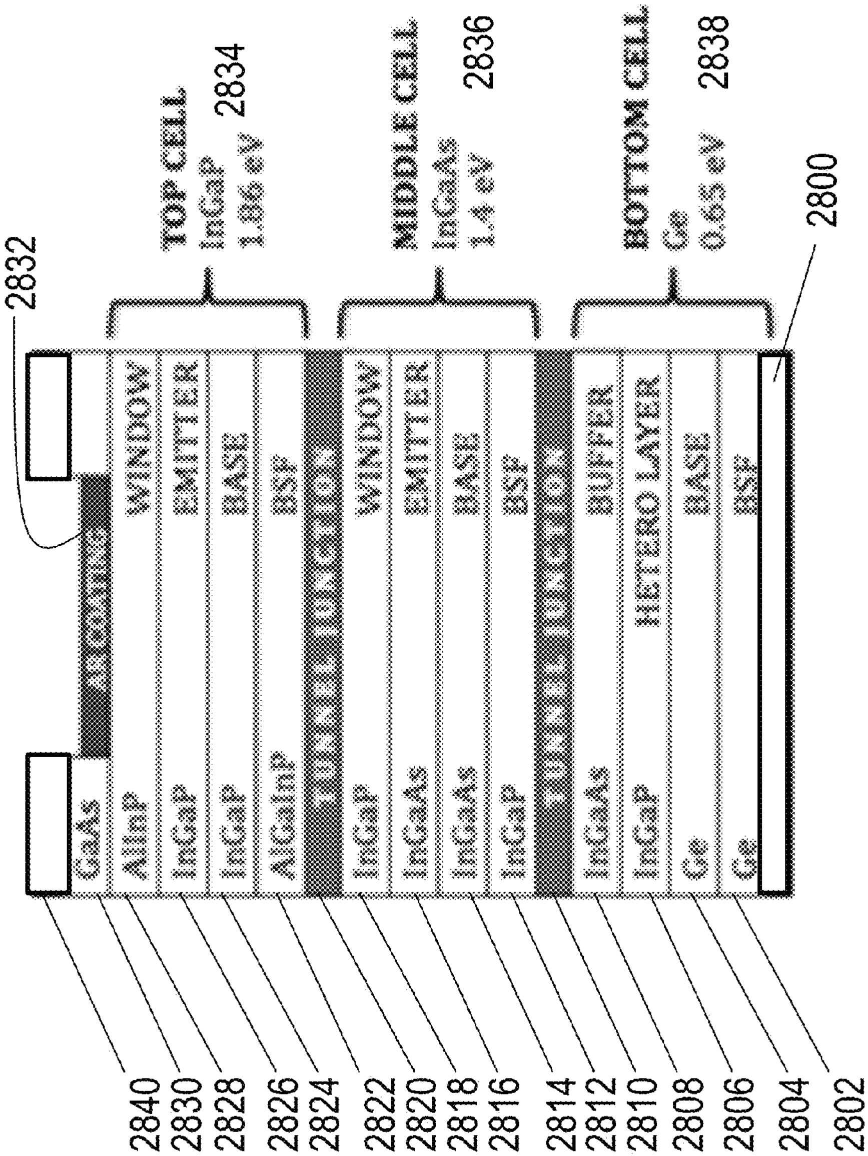


Fig. 28A (Prior art)

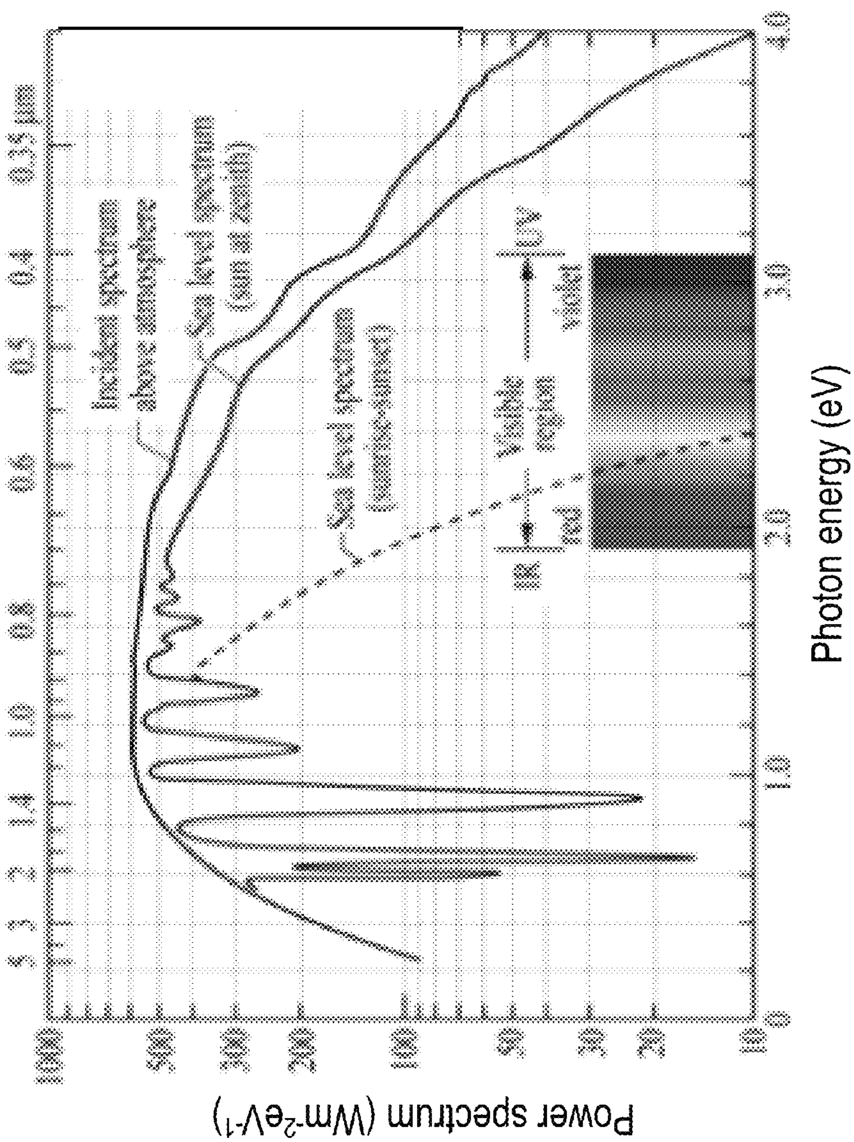

5
3
2
1.4
1.0
0.8
0.6
0.5
0.4
0.35 µm
Incident spectrum above atmosphere
Sea level spectrum (sun at zenith)
Sea level spectrum (sunrise+sunset)
IR
red
Visible region
violet
UV
1000
500
300
200
100
50
30
20
10
0
1.0
2.0
3.0
4.0
Photon energy (eV)
Power spectrum (Wm-2eV-1)

Fig. 28B

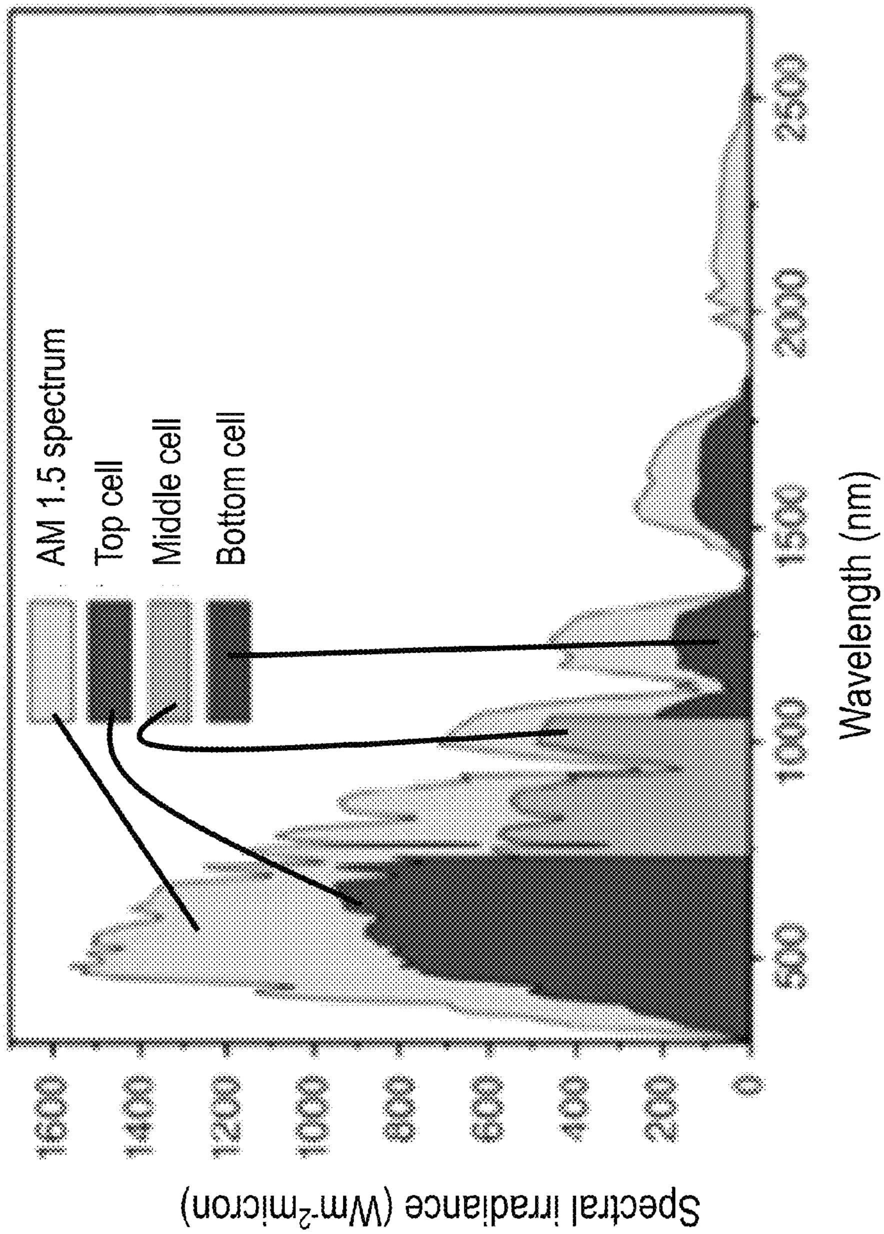
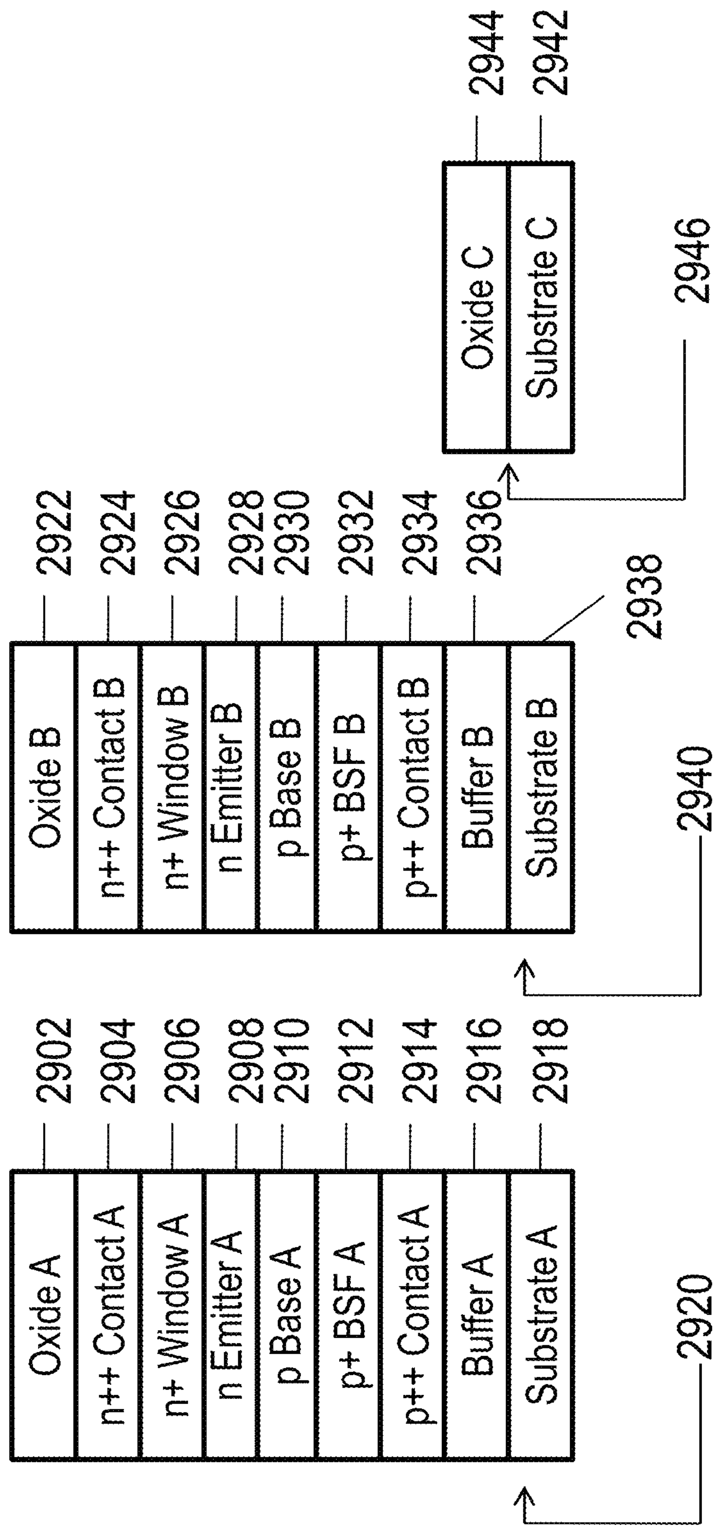

AM 1.5 spectrum
Top cell
Middle cell
Bottom cell
Spectral irradiance (Wm-2micron)
1600
1400
1200
1000
800
600
400
200
0
500
1000
1500
2000
2500
Wavelength (nm)

Fig. 28C



Oxide A
n++ Contact A
n+ Window A
n Emitter A
p Base A
p+ BSF A
p++ Contact A
Buffer A
Substrate A
2902
2904
2906
2908
2910
2912
2914
2916
2918
2920
Oxide B
n++ Contact B
n+ Window B
n Emitter B
p Base B
p+ BSF B
p++ Contact B
Buffer B
Substrate B
2922
2924
2926
2928
2930
2932
2934
2936
2938
2940
Oxide C
Substrate C
2944
2942
2946

Fig. 29A

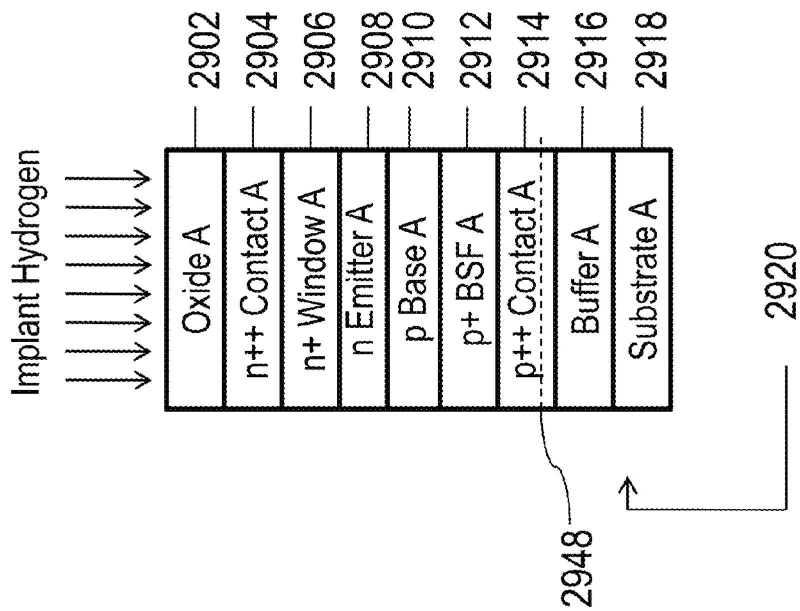

Implant Hydrogen
Oxide A
n++ Contact A
n+ Window A
n Emitter A
p Base A
p+ BSF A
p++ Contact A
Buffer A
Substrate A
2902
2904
2906
2908
2910
2912
2914
2916
2918
2920
2948

Fig. 29B

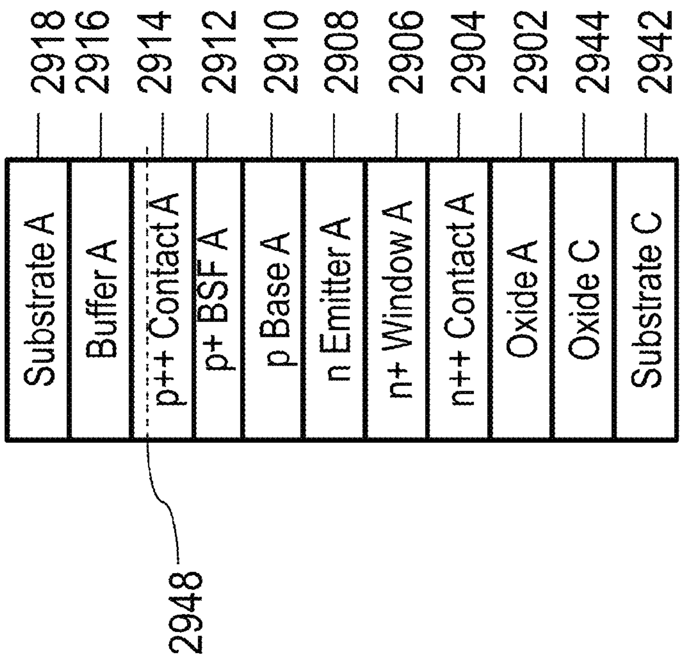

Substrate A
Buffer A
p++ Contact A
p+ BSF A
p Base A
n Emitter A
n+ Window A
n++ Contact A
Oxide A
Oxide C
Substrate C
2918
2916
2914
2912
2910
2908
2906
2904
2902
2944
2942
2948

Fig. 29C

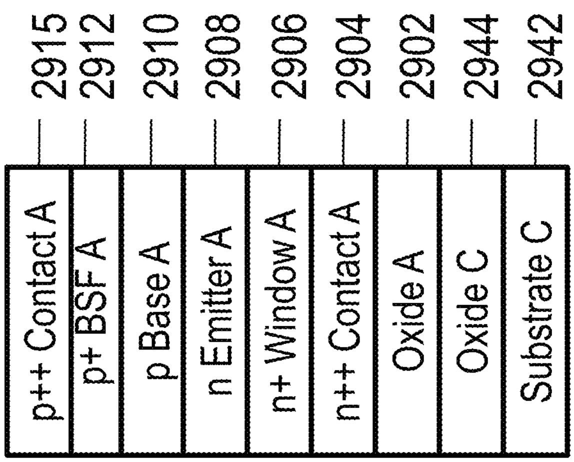

p++ Contact A
p+ BSF A
p Base A
n Emitter A
n+ Window A
n++ Contact A
Oxide A
Oxide C
Substrate C
2915
2912
2910
2908
2906
2904
2902
2944
2942

Fig. 29D

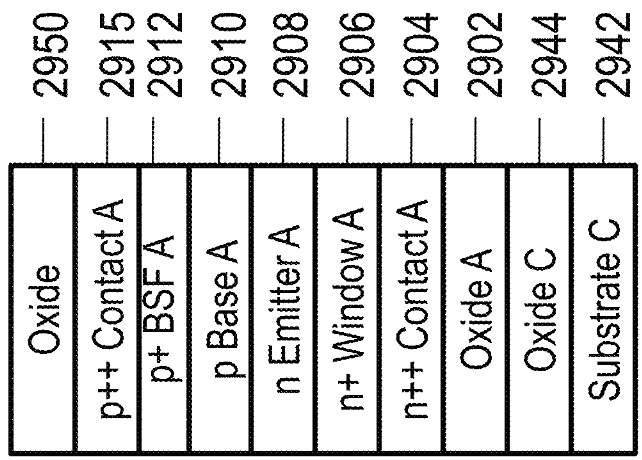

2950
2915
2912
2910
2908
2906
2904
2902
2944
2942
Oxide
p++ Contact A
p+ BSF A
p Base A
n Emitter A
n+ Window A
n++ Contact A
Oxide A
Oxide C
Substrate C

Fig. 29E

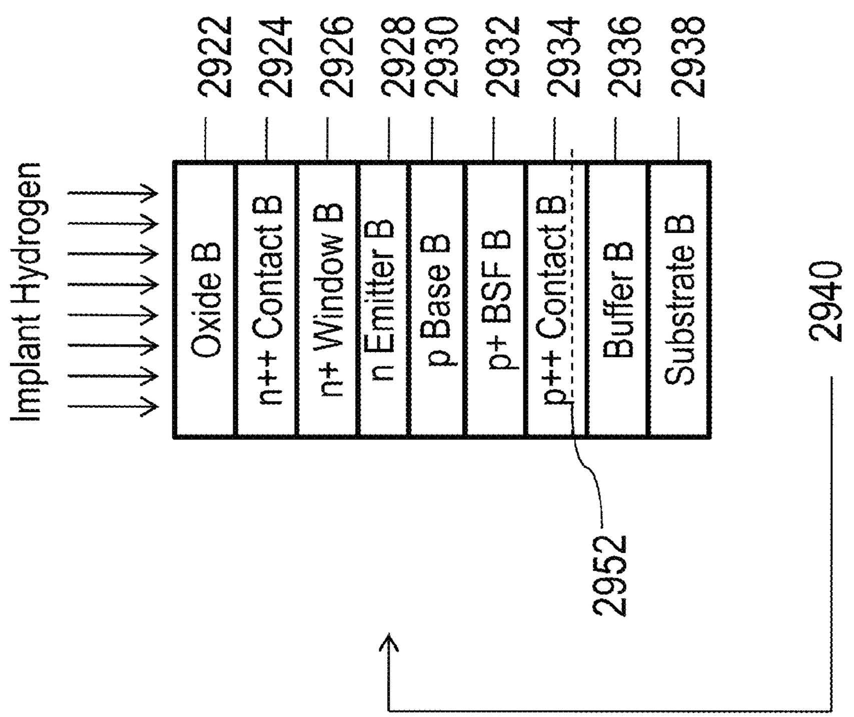
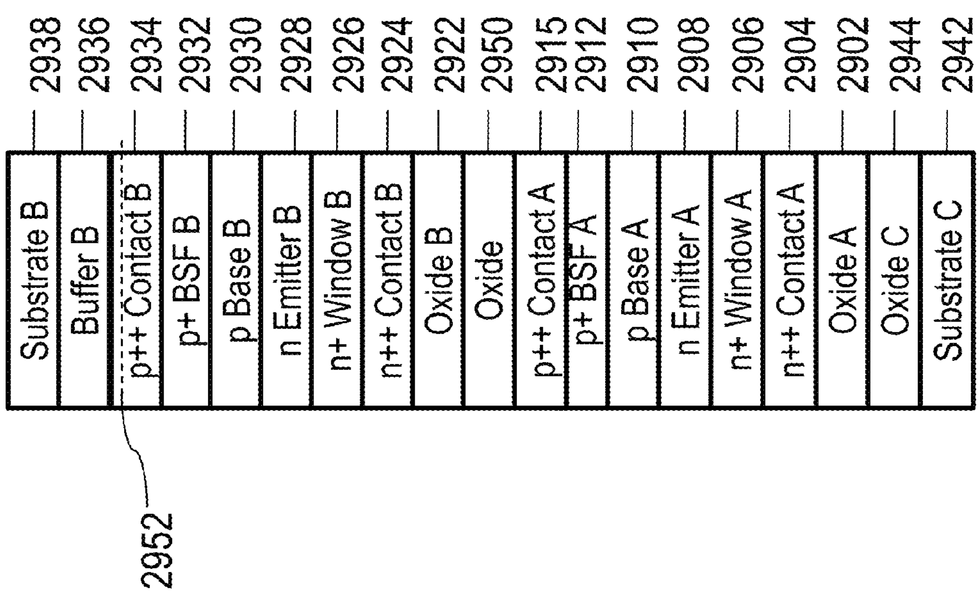

Implant Hydrogen
Oxide B
n++ Contact B
n+ Window B
n Emitter B
p Base B
p+ BSF B
p++ Contact B
Buffer B
Substrate B
2922
2924
2926
2928
2930
2932
2934
2936
2938
2952
2940

Fig. 29F

Fig. 29G


Substrate B
Buffer B
p++ Contact B
p+ BSF B
p Base B
n Emitter B
n+ Window B
n++ Contact B
Oxide B
Oxide
p++ Contact A
p+ BSF A
p Base A
n Emitter A
n+ Window A
n++ Contact A
Oxide A
Oxide C
Substrate C
2938
2936
2934
2932
2930
2928
2926
2924
2922
2950
2915
2912
2910
2908
2906
2904
2902
2944
2942
2952


Oxide 2954
p++ Contact B 2935
p+ BSF B 2932
p Base B 2930
n Emitter B 2928
n+ Window B 2926
n++ Contact B 2924
Oxide B 2922
Oxide 2950
p++ Contact A 2915
p+ BSF A 2912
p Base A 2910
n Emitter A 2908
n+ Window A 2906
n++ Contact A 2904
Oxide A 2902
Oxide C 2944
Substrate C 2942

Fig. 29H

Fig. 30A

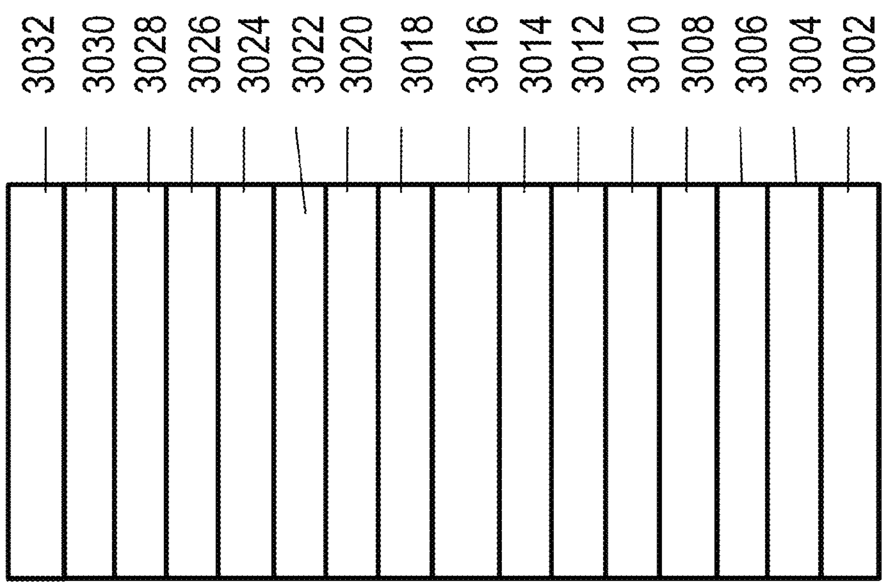

3032
3030
3028
3026
3024
3022
3020
3018
3016
3014
3012
3010
3008
3006
3004
3002

Fig. 30B

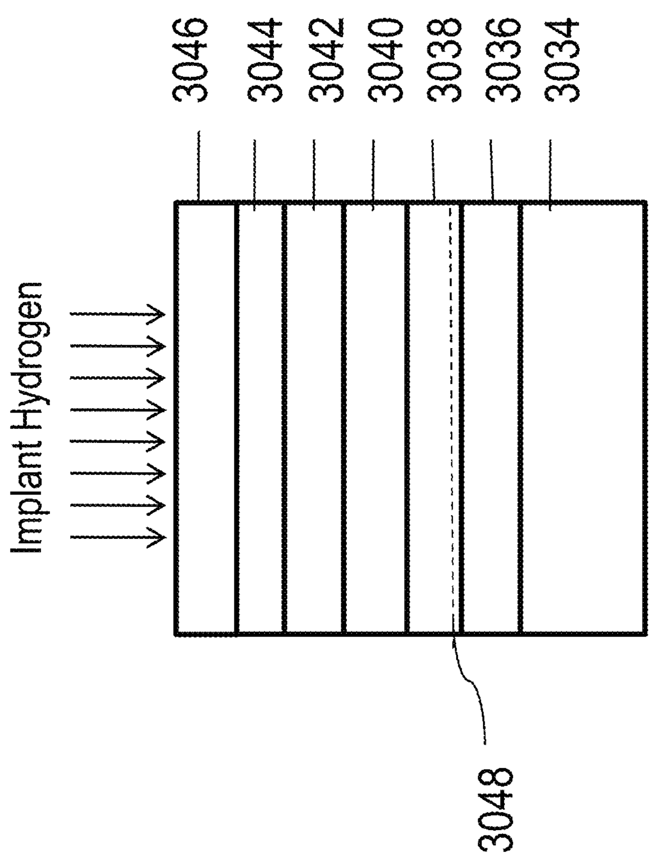


Fig. 30C

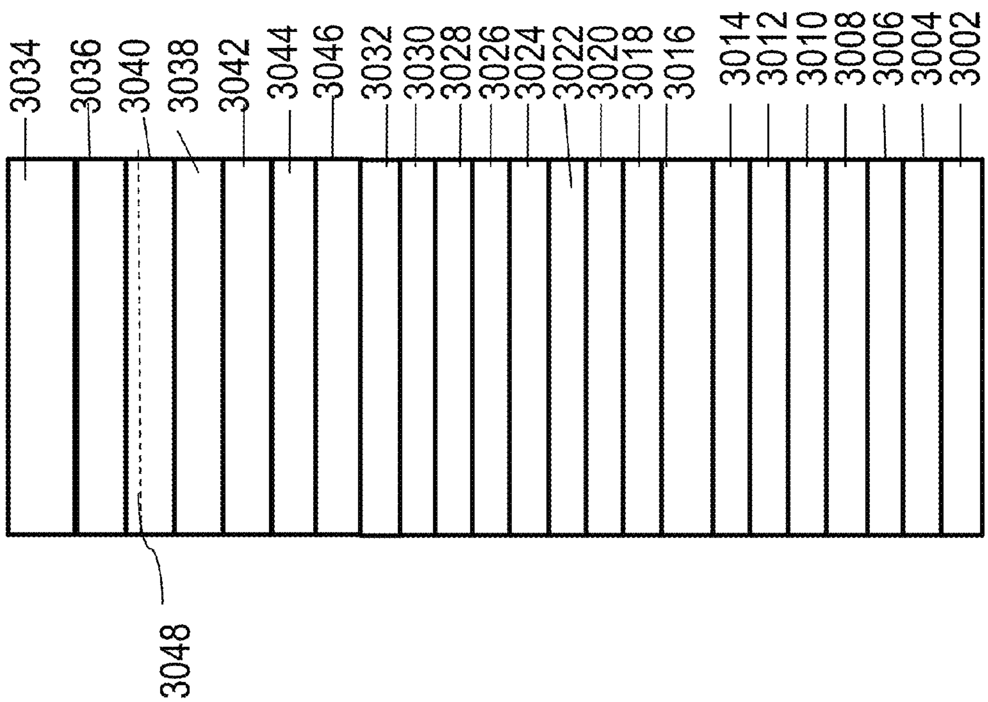
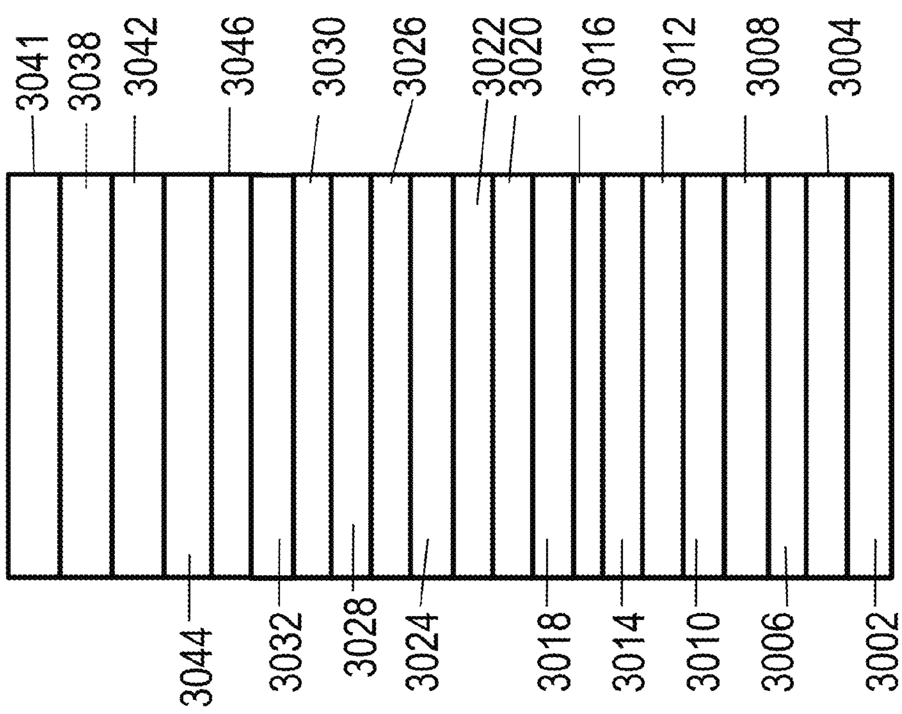

3034
3036
3040
3038
3042
3044
3046
3032
3030
3028
3026
3024
3022
3020
3018
3016
3014
3012
3010
3008
3006
3004
3002
3048

Fig. 30D


3041
3038
3042
3046
3030
3026
3022
3020
3016
3012
3008
3004
3044
3032
3028
3024
3018
3014
3010
3006
3002

SEMICONDUCTOR AND OPTOELECTRONIC DEVICES

CROSS-REFERENCE OF RELATED APPLICATION

This application is a continuation application of co-pending U.S. patent application Ser. No. 13/422,057, filed on Mar. 16, 2012, which is a continuation of U.S. patent application Ser. No. 12/904,103, filed on Oct. 13, 2010, now U.S. Pat. No. 8,163,581, the entire contents of the foregoing applications are incorporated by reference. Furthermore, priority is claimed to U.S. patent application Ser. No. 12/900,379, filed on Oct. 7, 2010, now U.S. Pat. No. 8,395,191 and U.S. patent application Ser. No. 13/273,712, filed on Oct. 14, 2011, now U.S. Pat. No. 8,273,610, the entire contents of the foregoing applications are incorporated by reference.

BACKGROUND OF THE INVENTION

(A) Field of the Invention

This invention describes applications of monolithic 3D integration to various disciplines, including but not limited to, for example, light-emitting diodes, displays, image-sensors and solar cells.

(B) Discussion of Background Art

Semiconductor and optoelectronic devices often require thin monocrystalline (or single-crystal) films deposited on a certain wafer. To enable this deposition, many techniques, generally referred to as layer transfer technologies, have been developed. These include:

- Ion-cut, variations of which are referred to as smart-cut, nano-cleave and smart-cleave: Further information on ion-cut technology is given in "Frontiers of silicon-on-insulator," J. Appl. Phys. 93, 4955-4978 (2003) by G. K. Celler and S. Cristolovean ("Celler") and also in "Mechanically induced Si layer transfer in hydrogen-implanted Si wafers," Appl. Phys. Lett., vol. 76, pp. 2370-2372, 2000 by K. Henttinen, I. Suni, and S. S. Lau ("Hentinnen").
- Porous silicon approaches such as ELTRAN: These are described in "Eltran, Novel SOI Wafer Technology", JSAP International, Number 4, July 2001 by T. Yonehara and K. Sakaguchi ("Yonehara").
- Lift-off with a temporary substrate, also referred to as epitaxial lift-off: This is described in "Epitaxial lift-off and its applications", 1993 Semicond. Sci. Technol. 8 1124 by P. Demeester, et al ("Demeester").
- Bonding a substrate with single crystal layers followed by Polishing, Time-controlled etch-back or Etch-stop layer controlled etch-back to thin the bonded substrate: These are described in U.S. Pat. No. 6,806,171 by A. Ulyashin and A. Usenko ("Ulyashin") and "Enabling SOI-Based Assembly Technology for Three-Dimensional (3D) Integrated Circuits (ICs)," IEDM Tech. Digest, p. 363 (2005) by A. W. Topol, D. C. La Tulipe, L. Shi, S. M. Alam, D. J. Frank, S. E. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, J. Patel, S. Goma, D. DiMilia, M. T. Robson, E. Duch, M. Farinelli, C. Wang, R. A. Conti, D. M. Canaperi, L. Deligianni, A. Kumar, K. T. Kwietniak, C. D'Emic, J. Ott, A. M. Young, K. W. Guarini, and M. Ieong ("Topol").
- Bonding a wafer with a Gallium Nitride film epitaxially grown on a sapphire substrate followed by laser lift-off for removing the transparent sapphire substrate: This method may be suitable for deposition of Gallium Nitride thin films, and is described in U.S. Pat. No. 6,071,795 by Nathan W. Cheung, Timothy D. Sands and William S. Wong ("Cheung").
- Rubber stamp layer transfer: This is described in "Solar cells sliced and diced", 19 May 2010, Nature News.

With novel applications of these methods and recognition of their individual strengths and weaknesses, one can significantly enhance today's light-emitting diode (LED), display, image-sensor and solar cell technologies.

Background on LEDs

Light emitting diodes (LEDs) are used in many applications, including automotive lighting, incandescent bulb replacements, and as backlights for displays. Red LEDs are typically made on Gallium Arsenide (GaAs) substrates, and include quantum wells constructed of various materials such as AlInGaP and GaInP. Blue and green LEDs are typically made on Sapphire or Silicon Carbide (SiC) or bulk Gallium Nitride (GaN) substrates, and include quantum wells constructed of various materials such as GaN and InGaN.

A white LED for lighting and display applications can be constructed by either using a blue LED coated with phosphor (called phosphor-coated LED or pcLED) or by combining light from red, blue, and green LEDs (called RGB LED). RGB LEDs are typically constructed by placing red, blue, and green LEDs side-by-side. While RGB LEDs are more energy-efficient than pcLEDs, they are less efficient in mixing red, blue and green colors to form white light. They also are much more costly than pcLEDs. To tackle issues with RGB LEDs, several proposals have been made.

One RGB LED proposal from Hong Kong University is described in "Design of vertically stacked polychromatic light emitting diodes", Optics Express, June 2009 by K. Hui, X. Wang, et al ("Hui"). It involves stacking red, blue, and green LEDs on top of each other after individually packaging each of these LEDs. While this solves light mixing problems, this RGB-LED is still much more costly than a pcLED solution since three LEDs for red, blue, and green color need to be packaged. A pcLED, on the other hand, requires just one LED to be packaged and coated with phosphor.

Another RGB LED proposal from Nichia Corporation is described in "Phosphor Free High-Luminous-Efficiency White Light-Emitting Diodes Composed of InGaN Multi-Quantum Well", Japanese Journal of Applied Physics, 2002 by M. Yamada, Y. Narukawa, et al. ("Yamada"). It involves constructing and stacking red, blue and green LEDs of GaN-based materials on a sapphire or SiC substrate. However, red LEDs are not efficient when constructed with GaN-based material systems, and that hampers usefulness of this implementation. It is not possible to deposit defect-free AlInGaP/InGaP for red LEDs on the same substrate as GaN based blue and green LEDs, due to a mismatch in thermal expansion co-efficient between the various material systems.

Yet another RGB-LED proposal is described in "Cascade Single chip phosphor-free while light emitting diodes", Applied Physics Letters, 2008 by X. Guo, G. Shen, et al. ("Guo"). It involves bonding GaAs based red LEDs with GaN based blue-green LEDs to produce white light. Unfortunately, this bonding process requires 600° C. temperatures, causing issues with mismatch of thermal expansion co-efficients and cracking. Another publication on this topic is "A trichromatic phosphor-free white light-emitting diode by using adhesive bonding scheme", Proc. SPIE, Vol. 7635, 2009 by D. Chuai, X. Guo, et al. ("Chuai"). It involves bonding red LEDs with green-blue LED stacks. Bonding is done at the die level after dicing, which is more costly than a wafer-based approach.

U.S. patent application Ser. No. 12/130,824 describes various stacked RGB LED devices. It also briefly mentions a method for construction of a stacked LED where all layers of the stacked LED are transferred using lift-off with a temporary carrier and Indium Tin Oxide (ITO) to semiconductor bonding. This method has several issues for constructing a RGB LED stack. First, it is difficult to manufacture a lift-off with a temporary carrier of red LEDs for producing a RGB LED stack, especially for substrates larger than 2 inch. This is because red LEDs are typically constructed on non-transparent GaAs substrates, and lift-off with a temporary carrier is done by using an epitaxial lift-off process. Here, the thin film to be transferred typically sits atop a "release-layer" (eg. AlAs), this release layer is removed by etch procedures after the thin film is attached to a temporary substrate. Scaling this process to 4 inch wafers and bigger is difficult. Second, it is very difficult to perform the bonding of ITO to semiconductor materials of a LED layer at reasonable temperatures, as described in the patent application Ser. No. 12/130,824.

It is therefore clear that a better method for constructing RGB LEDs will be helpful. Since RGB LEDs are significantly more efficient than pcLEDs, they can be used as replacements of today's phosphor-based LEDs for many applications, provided a cheap and effective method of constructing RGB LEDs can be invented.

Background on Image-Sensors:

Image sensors are used in applications such as cameras. Red, blue, and green components of the incident light are sensed and stored in digital format. CMOS image sensors typically contain a photodetector and sensing circuitry. Almost all image sensors today have both the photodetector and sensing circuitry on the same chip. Since the area consumed by the sensing circuits is high, the photodetector cannot see the entire incident light, and image capture is not as efficient.

To tackle this problem, several researchers have proposed building the photodetectors and the sensing circuitry on separate chips and stacking them on top of each other. A publication that describes this method is "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology", Intl. Solid State Circuits Conference 2005 by Suntharalingam, V., Berger, R., et al. ("Suntharalingam"). These proposals use through-silicon via (TSV) technology where alignment is done in conjunction with bonding. However, pixel size is reaching the 1 μm range, and successfully processing TSVs in the 1 μm range or below is very difficult. This is due to alignment issues while bonding. For example, the International Technology Roadmap for Semiconductors (ITRS) suggests that the 2-4 um TSV pitch will be the industry standard until 2012. A 2-4 μm pitch TSV will be too big for a sub-1 μm pixel. Therefore, novel techniques of stacking photodetectors and sensing circuitry are required.

A possible solution to this problem is given in "Setting up 3D Sequential Integration for Back-Illuminated CMOS Image Sensors with Highly Miniaturized Pixels with Low Temperature Fully-depleted SOI Transistors," IEDM, p. 1-4 (2008) by P. Coudrain et al. ("Coudrain"). In the publication, transistors are monolithically integrated on top of photodetectors. Unfortunately, transistor process temperatures reach 600° C. or more. This is not ideal for transistors (that require a higher thermal budget) and photodetectors (that may prefer a lower thermal budget).

Background on Displays:

Liquid Crystal Displays (LCDs) can be classified into two types based on manufacturing technology utilized: (1) Large-size displays that are made of amorphous/polycrystalline silicon thin-film-transistors (TFTs), and (2) Microdisplays that utilize single-crystal silicon transistors. Microdisplays are typically used where very high resolution is needed, such as camera/camcorder view-finders, projectors and wearable computers.

Microdisplays are made in semiconductor fabs with 200 mm or 300 mm wafers. They are typically constructed with LCOS (Liquid-Crystal-on-Silicon) Technology and are reflective in nature. An exception to this trend of reflective microdisplays is technology from Kopin Corporation (U.S. Pat. No. 5,317,236, filed December 1991). This company utilizes transmittive displays with a lift-off layer transfer scheme. Transmittive displays may be generally preferred for various applications.

While lift-off layer transfer schemes are viable for transmittive displays, they are frequently not used for semiconductor manufacturing due to yield issues. Therefore, other layer transfer schemes will be helpful. However, it is not easy to utilize other layer transfer schemes for making transistors in microdisplays. For example, application of "smart-cut" layer transfer to attach monocrystalline silicon transistors to glass is described in "Integration of Single Crystal Si TFTs and Circuits on a Large Glass Substrate", IEDM 2009 by Y. Takafuji, Y. Fukushima, K. Tomiyasu, et al. ("Takafuji"). Unfortunately, hydrogen is implanted through the gate oxide of transferred transistors in the process, and this degrades performance. Process temperatures are as high as 600° C. in this paper, and this requires costly glass substrates. Several challenges therefore need to be overcome for efficient layer transfer, and require innovation.

Background on Solar Cells:

Solar cells can be constructed of several materials such as, for example, silicon and compound semiconductors. The highest efficiency solar cells are typically multi-junction solar cells that are constructed of compound semiconductor materials. These multi-junction solar cells are typically constructed on a germanium substrate, and semiconductors with various band-gaps are epitaxially grown atop this substrate to capture different portions of the solar spectrum.

There are a few issues with standard multi-junction solar cells. Since multiple junctions are grown epitaxially above a single substrate (such as Germanium) at high temperature, materials used for different junctions are restricted to those that have lattice constants and thermal expansion co-efficients close to those of the substrate. Therefore, the choice of materials used to build junctions for multi-junction solar cells is limited. As a result, mostmulti-junction solar cells commercially available today cannot capture the full solar spectrum. Efficiency of the solar cell can be improved if a large band of the solar spectrum is captured. Furthermore, multi-junction solar cells today suffer from high cost of the substrate above which multiple junctions are epitaxially grown. Methods to build multi-junction solar cells that tackle both these issues will be helpful.

A method of making multi-junction solar cells by mechanically bonding two solar cells, one with a Germanium junction and another with a compound semiconductor junction is described in "Towards highly efficient 4-terminal mechanical photovoltaic stacks", III-Vs Review, Volume 19, Issue 7, September-October 2006 by Giovanni Flamand, Jef Poortmans ("Flamand"). In this work, the authors make the compound semiconductor junctions on a Germanium substrate epitaxially. They then etch away the entire Germanium substrate after bonding to the other substrate with the Germanium junction. The process uses two Germanium substrates, and is therefore expensive.

Techniques to create multi-junction solar cells with layer transfer have been described in "Wafer bonding and layer transfer processes for 4-junction high efficiency solar cells," *Photovoltaic Specialists Conference,* 2002. *Conference Record of the Twenty-Ninth IEEE*, vol., no., pp. 1039-1042, 19-24 May 2002 by Zahler, J. M.; Fontcuberta i Morral, A.; Chang-Geun Ahn; Atwater, H. A.; Wanlass, M. W.; Chu, C. and Iles, P. A. An anneal is used for ion-cut purposes, and this anneal is typically done at temperatures higher than 350-400° C. (if high bond strength is desired). When that happens, cracking and defects can be produced due to mismatch of co-efficients of thermal expansion between various layers in the stack. Furthermore, semiconductor layers are bonded together, and the quality of this bond not as good as oxide-to-oxide bonding, especially for lower process temperatures.

SUMMARY

Techniques to utilize layer transfer schemes such as ion-cut to form novel light emitting diodes (LEDs), CMOS image sensors, displays, microdisplays and solar cells are discussed.

In one aspect, an integrated device, the integrated device including a first crystalline layer covered by an oxide layer, a second crystalline layer overlying the oxide layer, wherein the first and second crystalline layers are image sensor layers, and the device includes a third crystalline layer, wherein the third crystalline layer includes single crystal transistors.

In another aspect, an integrated image sensor, the integrated image sensor including a first mono-crystal layer including a plurality of image sensor pixels and alignment marks, and an oxide layer overlaying and on top of the first mono-crystal layer, and a second mono-crystal layer including a plurality of second image sensor pixels aligned to the alignment marks, and the second mono-crystal layer overlaying the oxide layer, and a third mono-crystal layer, wherein the third mono-crystal layer includes a plurality of single crystal transistors aligned to the alignment marks.

In another aspect, an integrated device, the integrated device including a first mono-crystal layer including a plurality of single crystal transistors and alignment marks, and an overlaying oxide on top of the first mono-crystal layer, and a second mono-crystal layer overlaying the oxide, and wherein the second mono-crystal layer includes a plurality of image sensor pixels aligned to the alignment marks.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments of the present invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

FIGS. **1**A-B illustrate red, green and blue type LEDs (prior art);

FIG. **2** illustrates a conventional RGB LED where red, green, and blue LEDs are placed side-by-side (prior art);

FIG. **3** illustrates a prior-art phosphor-based LED (pcLED);

FIGS. **4**A-S illustrate an embodiment of this invention, where RGB LEDs are stacked with ion-cut technology, flip-chip packaging and conductive oxide bonding;

FIGS. **5**A-Q illustrate an embodiment of this invention, where RGB LEDs are stacked with ion-cut technology, wire bond packaging and conductive oxide bonding;

FIGS. **6**A-L illustrate an embodiment of this invention, where stacked RGB LEDs are formed with ion-cut technology, flip-chip packaging and aligned bonding;

FIGS. **7**A-L illustrate an embodiment of this invention, where stacked RGB LEDs are formed with laser lift-off, substrate etch, flip-chip packaging and conductive oxide bonding;

FIGS. **8**A-B illustrate an embodiment of this invention, where stacked RGB LEDs are formed from a wafer having red LED layers and another wafer having both green and blue LED layers;

FIG. **9** illustrates an embodiment of this invention, where stacked RGB LEDs are formed with control and driver circuits for the LED built on the silicon sub-mount;

FIG. **10** illustrates an embodiment of this invention, where stacked RGB LEDs are formed with control and driver circuits as well as image sensors for the LED built on the silicon sub-mount;

FIGS. **11**A-F is a prior art illustration of pcLEDs constructed with ion-cut processes;

FIGS. **12**A-F illustrate an embodiment of this invention, where pcLEDs are constructed with ion-cut processes;

FIG. **13** illustrates a prior art image sensor stacking technology where connections between chips are aligned during bonding;

FIG. **14** describes two configurations for stacking photodetectors and read-out circuits;

FIGS. **15**A-H illustrate an embodiment of this invention, where a CMOS image sensor is formed by stacking a photodetector monolithically on top of read-out circuits using ion-cut technology;

FIG. **16** illustrates the absorption process of different wavelengths of light at different depths in silicon image sensors;

FIGS. **17**A-B illustrate an embodiment of this invention, where red, green and blue photodetectors are stacked monolithically atop read-out circuits using ion-cut technology (for an image sensor);

FIGS. **18**A-B illustrate an embodiment of this invention, where red, green and blue photodetectors are stacked monolithically atop read-out circuits using ion-cut technology for a different configuration (for an image sensor);

FIGS. **19**A-B illustrate an embodiment of this invention, where an image sensor that can detect both visible and infrared light without any loss of resolution is constructed;

FIG. **20**A illustrates an embodiment of this invention, where polarization of incoming light is detected;

FIG. **20**B illustrates another embodiment of this invention, where an image sensor with high dynamic range is constructed;

FIG. **21** illustrates an embodiment of this invention, where read-out circuits are constructed monolithically above photodetectors in an image sensor;

FIGS. **22**A-G illustrate an embodiment of this invention, where a display is constructed using sub-400° C. processed single crystal silicon recessed channel transistors on a glass substrate;

FIGS. **23**A-H illustrate an embodiment of this invention, where a display is constructed using sub-400° C. processed single crystal silicon replacement gate transistors on a glass substrate;

FIGS. **24**A-F illustrate an embodiment of this invention, where a display is constructed using sub-400° C. processed single crystal junctionless transistors on a glass substrate;

FIGS. **25**A-D illustrate an embodiment of this invention, where a display is constructed using sub-400° C. processed amorphous silicon or polysilicon junctionless transistors on a glass substrate;

FIGS. **26**A-C illustrate an embodiment of this invention, where a microdisplay is constructed using stacked RGB LEDs and control circuits are connected to each pixel with solder bumps;

FIGS. **27**A-D illustrate an embodiment of this invention, where a microdisplay is constructed using stacked RGB LEDs and control circuits are monolithically stacked above the LED;

FIGS. **28**A-C illustrate a description of multijunction solar cells (prior art);

FIGS. **29**A-H illustrate an embodiment of this invention, where multijunction solar cells are constructed using sub-250° C. bond and cleave processes; and

FIGS. **30**A-D illustrate an embodiment of this invention, where a full-spectrum multi-junction solar cells is constructed using sub-250° C. bond and cleave processes.

DETAILED DESCRIPTION

Embodiments of the present invention are now described with reference to FIGS. **1-30**, it being appreciated that the figures illustrate the subject matter not to scale or to measure.

NuLED Technology:

FIG. **1**A illustrates a cross-section of prior art red LEDs. Red LEDs are typically constructed on a Gallium Arsenide substrate **100**. Alternatively, Gallium Phosphide or some other material can be used for the substrate. Since Gallium Arsenide **100** is opaque, a Bragg Reflector **101** is added to ensure light moves in the upward direction. Red light is produced by a p-n junction with multiple quantum wells (MQW). A p-type confinement layer **104**, a n-type confinement layer **102** and a multiple quantum well **103** form this part of the device. A current spreading region **105** ensures current flows throughout the whole device and not just close to the contacts. Indium Tin Oxide (ITO) could be used for the current spreading region **105**. A top contact **106** and a bottom contact **107** are used for making connections to the LED. It will be obvious to one skilled in the art based on the present disclosure that many configurations and material combinations for making red LEDs are possible. This invention is not limited to one particular configuration or set of materials.

FIG. **1**B also illustrates green and blue LED cross-sections. These are typically constructed on a sapphire, SiC or bulk-GaN substrate, indicated by **108**. Light is produced by a p-n junction with multiple quantum wells made of $In_xGa_{1-x}N$/GaN. A p-type confinement layer **111**, a n-type confinement layer **109** and a multiple quantum well **110** form this part of the device. The value of subscript x in $In_xGa_{1-x}N$ determines whether blue light or green light is produced. For example, blue light typically corresponds to x ranging from 10% to 20% while green light typically corresponds to x ranging from 20% to 30%. A current spreader **112** is typically used as well. ITO could be a material used for the current spreader **112**. An alternative material for current spreading could be ZnO. A top contact **113** and a bottom contact **114** are used for making connections to the LED. It will be obvious to one skilled in the art based on the present disclosure that many configurations and material combinations for making blue and green LEDs are possible. This invention is not limited to one particular configuration or set of materials.

White LEDs for various applications can be constructed in two ways. Method **1** is described in FIG. **2** which shows Red LED **201**, blue LED **202**, and green LED **203** that are constructed separately and placed side-by-side. Red light **204**, blue light **205** and green light **206** are mixed to form white light **207**. While these "RGB LEDs" are efficient, they suffer from cost issues and have problems related to light mixing. Method **2** is described in FIG. **3** which shows a blue LED **301** constructed and coated with a phosphor layer **302**. The yellow phosphor layer converts blue light into white light **303**. These "Phosphor-based LEDs" or "pcLEDs" are cheaper than RGB LEDs but are typically not as efficient.

FIG. **4**A-S illustrate an embodiment of this invention where Red, Blue, and Green LEDs are stacked on top of each other with smart layer transfer techniques. A smart layer transfer may be defined as one or more of the following processes:

- Ion-cut, variations of which are referred to as smart-cut, nano-cleave and smart-cleave: Further information on ion-cut technology is given in "Frontiers of silicon-on-insulator," J. Appl. Phys. 93, 4955-4978 (2003) by G. K. Celler and S. Cristolovean ("Celler") and also in "Mechanically induced Si layer transfer in hydrogen-implanted Si wafers," Appl. Phys. Lett., vol. 76, pp. 2370-2372, 2000 by K. Henttinen, I. Suni, and S. S. Lau ("Hentinnen").
- Porous silicon approaches such as ELTRAN: These are described in "Eltran, Novel SOI Wafer Technology," JSAP International, Number 4, July 2001 by T. Yonehara and K. Sakaguchi ("Yonehara").
- Bonding a substrate with single crystal layers followed by Polishing, Time-controlled etch-back or Etch-stop layer controlled etch-back to thin the bonded substrate: These are described in U.S. Pat. No. 6,806,171 by A. Ulyashin and A. Usenko ("Ulyashin") and "Enabling SOI-Based Assembly Technology for Three-Dimensional (3D) Integrated Circuits (ICs)," IEDM Tech. Digest, p. 363 (2005) by A. W. Topol, D. C. La Tulipe, L. Shi, S. M. Alam, D. J. Frank, S. E. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, J. Patel, S. Goma, D. DiMilia, M. T. Robson, E. Duch, M. Farinelli, C. Wang, R. A. Conti, D. M. Canaperi, L. Deligianni, A. Kumar, K. T. Kwietniak, C. D'Emic, J. Ott, A. M. Young, K. W. Guarini, and M. Ieong ("Topol").
- Bonding a wafer with a Gallium Nitride film epitaxially grown on a sapphire substrate followed by laser lift-off for removing the transparent sapphire substrate: This method may be suitable for deposition of Gallium Nitride thin films, and is described in U.S. Pat. No. 6,071,795 by Nathan W. Cheung, Timothy D. Sands and William S. Wong ("Cheung").
- Rubber stamp layer transfer: This is described in "Solar cells sliced and diced," 19 May 2010, Nature News.

This process of constructing RGB LEDs could include several steps that occur in a sequence from Step (A) to Step (S). Many of them share common characteristics, features, modes of operation, etc. When the same reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **4**A. A red LED wafer **436** is constructed on a GaAs substrate **402** and includes a N-type confinement layer **404**, a multiple quantum well (MQW) **406**, a P-type confinement layer **408**, an optional reflector **409** and an ITO current spreader **410**. Examples of materials used to construct these layers, include, but are not limited to, doped AlInGaP for the N-type confinement layer **404** and P-type confinement layer **408**, the multiple quantum well layer **406** could be of AlInGaP and GaInP and the optional reflector **409** could be a distributed Bragg Reflector. A double heterostructure configuration or single quantum well configuration could be used instead of a multiple quantum well configuration. Various other material types and configurations could be used for constructing the red LEDs for this process. Yet another wafer is constructed with a green LED. The green LED wafer **438** is constructed on a sapphire or SiC or bulk-GaN substrate **412** and includes a N-type confinement layer **414**, a multiple quantum well (MQW) **416**, a buffer layer **418**, a P-type confinement layer **420**, an optional reflector **421** and an ITO current spreader **422**. Yet another wafer is constructed with a blue LED. The blue LED wafer **440** is constructed on a sapphire or SiC or bulk-GaN substrate **424** and includes a N-type confinement layer **426**, a multiple quantum well (MQW) **428**, a buffer layer **430**, a P-type confinement layer **432**, an optional reflector **433** and an ITO current spreader **434**. Examples of materials used to construct these blue and green LED layers, include, but are not limited to, doped GaN for the N-type and P-type confinement layers **414**, **420**, **426** and **432**, AlGaN for the buffer layers **430** and **418** and InGaN/GaN for the multiple quantum wells **416** and **428**. The optional reflectors **421** and **433** could be distributed Bragg Reflectors or some other type of reflectors. Various other material types and configurations could be used for constructing blue and green LEDs for this process.

Step (B) is illustrated in FIG. **4**B. The blue LED wafer **440** from FIG. **4**A is used for this step. Various elements in FIG. **4**B such as, for example, **424**, **426**, **428**, **430**, **432**, **433**, and **434** have been previously described. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines **442**. Alternatively, helium could be used for this step.

Step (C) is illustrated in FIG. **4**C. A glass substrate **446** is taken and an ITO layer **444** is deposited atop it.

Step (D) is illustrated in FIG. **4**D. The wafer shown in FIG. **4**B is flipped and bonded atop the wafer shown in FIG. **4**C using ITO-ITO bonding. Various elements in FIG. **4**D such as **424**, **426**, **428**, **430**, **432**, **433**, **434**, **442**, **446**, and **444** have been previously described. The ITO layer **444** is essentially bonded to the ITO layer **434** using an oxide-to-oxide bonding process.

Step (E) is illustrated in FIG. **4**E. Various elements in FIG. **4**E such as **424**, **426**, **428**, **430**, **432**, **433**, **434**, **442**, **446**, and **444** have been previously described. An ion-cut process is conducted to cleave the structure shown in FIG. **4**D at the hydrogen implant plane **442**. This ion-cut process may use a mechanical cleave. An anneal process could be utilized for the cleave as well. After the cleave, a chemical mechanical polish (CMP) process is conducted to planarize the surface. The N-type confinement layer present after this cleave and CMP process is indicated as **427**.

Step (F) is illustrated in FIG. **4**F. Various elements in FIG. **4**F such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, and **427** have been previously described. An ITO layer **448** is deposited atop the N-type confinement layer **427**.

Step (G) is illustrated in FIG. **4**G. The green LED wafer **438** shown in Step (A) is used for this step. Various elements in FIG. **4**G such as **412**, **414**, **416**, **418**, **420**, **421**, and **422** have been described previously. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines **450**. Alternatively, helium could be used for this step.

Step (H) is illustrated in FIG. **4**H. The structure shown in FIG. **4**G is flipped and bonded atop the structure shown in FIG. **4**F using ITO-ITO bonding. Various elements in FIG. **4**H such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **412**, **414**, **416**, **418**, **420**, **421**, **422**, and **450** have been described previously.

Step (I) is illustrated in FIG. **4**I. The structure shown in FIG. **4**H is cleaved at the hydrogen plane indicated by **450**. This cleave process may be preferably done with a mechanical force. Alternatively, an anneal could be used. A CMP process is conducted to planarize the surface. Various elements in FIG. **4**I such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, and **422** have been described previously. The N-type confinement layer present after this cleave and CMP process is indicated as **415**.

Step (J) is illustrated in FIG. **4**J. An ITO layer **452** is deposited atop the structure shown in FIG. **4**I. Various elements in FIG. **4**J such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, and **422** have been described previously.

Step (K) is illustrated in FIG. **4**K. The red LED wafer **436** shown in Step (A) is used for this step. Various elements in FIG. **4**K such as **402**, **404**, **406**, **408**, **409**, and **410** have been described previously. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines **454**. Alternatively, helium could be used for this step.

Step (L) is illustrated in FIG. **4**L. The structure shown in FIG. **4**K is flipped and bonded atop the structure shown in FIG. **4**J using ITO-ITO bonding. Various elements in FIG. **4**L such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **402**, **404**, **406**, **408**, **409**, **410**, and **454** have been described previously.

Step (M) is illustrated in FIG. **4**M. The structure shown in FIG. **4**L is cleaved at the hydrogen plane **454**. A mechanical force could be used for this cleave. Alternatively, an anneal could be used. A CMP process is then conducted to planarize the surface. The N-type confinement layer present after this process is indicated as **405**. Various elements in FIG. **4**M such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, and **410** have been described previously.

Step (N) is illustrated in FIG. **4**N. An ITO layer **456** is deposited atop the structure shown in FIG. **4**M. Various elements in FIG. **4**M such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, **410**, and **405** have been described previously.

Step (O) is illustrated in FIG. **4**O. A reflecting material layer **458**, constructed for example with Aluminum or Silver, is deposited atop the structure shown in FIG. **4**N. Various elements in FIG. **4**O such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, **410**, **456**, and **405** have been described previously.

Step (P) is illustrated in FIG. **4**P. The process of making contacts to various layers and packaging begins with this step. A contact and bonding process similar to the one used in "High-power AlGaInN flip-chip light-emitting diodes," *Applied Physics Letters*, vol. 78, no. 22, pp. 3379-3381, May 2001, by Wierer, J. J.; Steigerwald, D. A.; Krames, M. R.; OShea, J. J.; Ludowise, M. J.; Christenson, G.; Shen, Y.-C.; Lowery, C.; Martin, P. S.; Subramanya, S.; Gotz, W.; Gardner, N. F.; Kern, R. S.; Stockman, S. A. is used. Vias **460** are etched to different layers of the LED stack. Various elements in FIG. **4**P such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, **410**, **456**, **405**, and **458** have been described previously. After the via holes **460** are etched, they may optionally be filled with an oxide layer and polished with CMP. This fill with oxide may be optional, and the preferred process may be to leave the via holes as such without fill. Note that the term contact holes could be used instead of the term via holes. Similarly, the term contacts could be used instead of the term vias.

Step (Q) is illustrated in FIG. **4**Q. Aluminum is deposited to fill via holes **460** from FIG. **4**P. Following this deposition, a lithography and etch process is utilized to define the aluminum metal to form vias **462**. The vias **462** are smaller in diameter than the via holes **460** shown in FIG. **4**P. Various elements in FIG. **4**Q such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, **410**, **456**, **405**, **460**, and **458** have been described previously.

Step (R) is illustrated in FIG. **4**R. A nickel layer **464** and a solder layer **466** are formed using standard procedures. Various elements in FIG. **4**R such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, **410**, **456**, **405**, **460**, **462**, and **458** have been described previously.

Step (S) is illustrated in FIG. **4**S. The solder layer **466** is then bonded to pads on a silicon sub-mount **468**. Various elements in FIG. **4**S such as **446**, **444**, **434**, **433**, **432**, **430**, **428**, **427**, **448**, **416**, **418**, **420**, **421**, **415**, **422**, **452**, **406**, **408**, **409**, **410**, **456**, **405**, **460**, **462**, **458**, **464**, and **466** have been described previously. The configuration of optional reflectors **433**, **421**, and **409** determines light output coming from the LED. A preferred embodiment of this invention may not have a reflector **433**, and may have the reflector **421** (reflecting only the blue light produced by multiple quantum well **428**) and the reflector **409** (reflecting only the green light produced by multiple quantum well **416**). In the process described in FIG. **4**A-FIG. **4**S, the original substrates in FIG. **4**A, namely **402**, **412** and **424**, can be reused after ion-cut. This reuse may make the process more cost-effective.

FIGS. **5**A-Q describe an embodiment of this invention, where RGB LEDs are stacked with ion-cut technology, wire bond packaging and conductive oxide bonding. Essentially, smart-layer transfer is utilized to construct this embodiment of the invention. This process of constructing RGB LEDs could include several steps that occur in a sequence from Step (A) to Step (Q). Many of the steps share common characteristics, features, modes of operation, etc. When the same reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A): This is illustrated using FIG. **5**A. A red LED wafer **536** is constructed on a GaAs substrate **502** and includes a N-type confinement layer **504**, a multiple quantum well (MQW) **506**, a P-type confinement layer **508**, an optional reflector **509** and an ITO current spreader **510**. Examples of materials used to construct these layers, include, but are not limited to, doped AlInGaP for the N-type confinement layer **504** and P-type confinement layer **508**, the multiple quantum well layer **506** could be of AlInGaP and GaInP and the optional reflector **509** could be a distributed Bragg Reflector. A double heterostructure configuration or single quantum well configuration could be used instead of a multiple quantum well configuration. Various other material types and configurations could be used for constructing the red LEDs for this process. Yet another wafer is constructed with a green LED. The green LED wafer **538** is constructed on a sapphire or SiC or bulk-GaN substrate **512** and includes a N-type confinement layer **514**, a multiple quantum well (MQW) **516**, a buffer layer **518**, a P-type confinement layer **520**, an optional reflector **521** and an ITO current spreader **522**. Yet another wafer is constructed with a blue LED. The blue LED wafer **540** is constructed on a sapphire or SiC or bulk-GaN substrate **524** and includes a N-type confinement layer **526**, a multiple quantum well (MQW) **528**, a buffer layer **530**, a P-type confinement layer **532**, an optional reflector **533** and an ITO current spreader **534**. Examples of materials used to construct these blue and green LED layers, include, but are not limited to, doped GaN (for the N-type and P-type confinement layers **514**, **520**, **526**, and **532**), AlGaN (for the buffer layers **530** and **518**), and InGaN/GaN (for the multiple quantum wells **516** and **528**). The optional reflectors **521** and **533** could be distributed Bragg Reflectors or some other type of reflectors. Various other material types and configurations could be used for constructing blue and green LEDs for this process.

Step (B) is illustrated in FIG. **5**B. The red LED wafer **536** from FIG. **5**A is used for this step. Various elements in FIG. **5**B such as **502**, **504**, **506**, **508**, **509**, and **510** have been previously described. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines **542**. Alternatively, helium could be used for this step.

Step (C) is illustrated in FIG. **5**C. A silicon substrate **546** is taken and an ITO layer **544** is deposited atop it.

Step (D) is illustrated in FIG. **5**D. The wafer shown in FIG. **5**B is flipped and bonded atop the wafer shown in FIG. **5**C using ITO-ITO bonding. Various elements in FIG. **5**D such as **502**, **504**, **506**, **508**, **509**, **510**, **542**, **544**, and **546** have been previously described. The ITO layer **544** is essentially bonded to the ITO layer **510** using an oxide-to-oxide bonding process.

Step (E) is illustrated in FIG. **5**E. Various elements in FIG. **5**E such as **506**, **508**, **509**, **510**, **544** and **546** have been previously described. An ion-cut process is conducted to cleave the structure shown in FIG. **5**D at the hydrogen implant plane **542**. This ion-cut process could preferably use a mechanical cleave. An anneal process could be utilized for the cleave as well. After the cleave, a chemical mechanical polish (CMP) process is conducted to planarize the surface. The N-type confinement layer present after this cleave and CMP process is indicated as **505**.

Step (F) is illustrated in FIG. **5**F. Various elements in FIG. **5**F such as **505**, **506**, **508**, **509**, **510**, **544**, and **546** have been previously described. An ITO layer **548** is deposited atop the N-type confinement layer **505**.

Step (G) is illustrated in FIG. **5**G. The green LED wafer **538** shown in Step (A) is used for this step. Various elements in FIG. **5**G such as **512**, **514**, **516**, **518**, **520**, **521**, and **522** have been described previously. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines **550**. Alternatively, helium could be used for this step.

Step (H) is illustrated in FIG. **5**H. The structure shown in FIG. **5**G is flipped and bonded atop the structure shown in FIG. **5**F using ITO-ITO bonding. Various elements in FIG. **5**H such as **505**, **506**, **508**, **509**, **510**, **544**, **546**, **548**, **512**, **514**, **516**, **518**, **520**, **521**, **550**, and **522** have been described previously.

Step (I) is illustrated in FIG. **5**I. The structure shown in FIG. **5**H is cleaved at the hydrogen plane indicated by **550**. This cleave process may be preferably done with a mechanical force. Alternatively, an anneal could be used. A CMP process is conducted to planarize the surface. Various elements in FIG. **5**I such as **505**, **506**, **508**, **509**, **510**, **544**, **546**, **548**, **516**, **518**, **520**, **521**, and **522** have been described previously. The N-type confinement layer present after this cleave and CMP process is indicated as **515**.

Step (J) is illustrated using FIG. **5**J. An ITO layer **552** is deposited atop the structure shown in FIG. **5**I. Various elements in FIG. **5**J such as **505**, **506**, **508**, **509**, **510**, **544**, **546**, **548**, **516**, **518**, **520**, **521**, **515**, and **522** have been described previously.

Step (K) is illustrated using FIG. **5**K. The blue LED wafer **540** from FIG. **5**A is used for this step. Various elements in FIG. **5**K such as **524**, **526**, **528**, **530**, **532**, **533**, and **534** have been previously described. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines **554**. Alternatively, helium could be used for this step.

Step (L) is illustrated in FIG. **5**L. The structure shown in FIG. **5**K is flipped and bonded atop the structure shown in FIG. **5**J using ITO-ITO bonding. Various elements in FIG. **4**L such as **505**, **506**, **508**, **509**, **510**, **544**, **546**, **548**, **516**, **518**, **520**, **521**, 515, 522, 552, 524, 526, 528, 530, 532, 533, 554, and 534 have been described previously.

Step (M) is illustrated in FIG. 5M. The structure shown in FIG. 5L is cleaved at the hydrogen plane 554. A mechanical force could be used for this cleave. Alternatively, an anneal could be used. A CMP process is then conducted to planarize the surface. The N-type confinement layer present after this process is indicated as 527. Various elements in FIG. 5M such as 505, 506, 508, 509, 510, 544, 546, 548, 516, 518, 520, 521, 515, 522, 552, 528, 530, 532, 533, and 534 have been described previously.

Step (N) is illustrated in FIG. 5N. An ITO layer 556 is deposited atop the structure shown in FIG. 5M. Various elements in FIG. 5N such as 505, 506, 508, 509, 510, 544, 546, 548, 516, 518, 520, 521, 515, 522, 552, 528, 530, 532, 533, and 534 have been described previously.

Step (O) is illustrated in FIG. 5O. The process of making contacts to various layers and packaging begins with this step. Various elements in FIG. 5O such as 505, 506, 508, 509, 510, 544, 546, 548, 516, 518, 520, 521, 515, 522, 552, 528, 530, 532, 533, 556, and 534 have been described previously. Via holes 560 are etched to different layers of the LED stack. After the via holes 560 are etched, they may optionally be filled with an oxide layer and polished with CMP. This fill with oxide may be optional, and the preferred process may be to leave the via holes as such without fill.

Step (P) is illustrated in FIG. 5P. Aluminum is deposited to fill via holes 560 from FIG. 5O. Following this deposition, a lithography and etch process is utilized to define the aluminum metal to form via holes 562. Various elements in FIG. 5P such as 505, 506, 508, 509, 510, 544, 546, 548, 516, 518, 520, 521, 515, 522, 552, 528, 530, 532, 533, 556, 560, and 534 have been described previously.

Step (Q) is illustrated in FIG. 5Q. Bond pads 564 are constructed and wire bonds are attached to these bond pads following this step. Various elements in FIG. 5Q such as 505, 506, 508, 509, 510, 544, 546, 548, 516, 518, 520, 521, 515, 522, 552, 528, 530, 532, 533, 556, 560, 562, and 534 have been described previously. The configuration of optional reflectors 533, 521 and 509 determines light output coming from the LED. The preferred embodiment of this invention is to have reflector 533 reflect only blue light produced by multiple quantum well 528, to have the reflector 521 reflecting only green light produced by multiple quantum well 516 and to have the reflector 509 reflect light produced by multiple quantum well 506. In the process described in FIG. 5A-FIG. 5Q, the original substrates in FIG. 5A, namely 502, 512 and 524, can be re-used after ion-cut. This may make the process more cost-effective.

FIGS. 6A-L show an alternative embodiment of this invention, where stacked RGB LEDs are formed with ion-cut technology, flip-chip packaging and aligned bonding. A smart layer transfer process, ion-cut, is therefore utilized. This process of constructing RGB LEDs could include several steps that occur in a sequence from Step (A) to Step (K). Many of the steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. 6A. A red LED wafer 636 is constructed on a GaAs substrate 602 and includes a N-type confinement layer 604, a multiple quantum well (MQW) 606, a P-type confinement layer 608, an optional reflector 609 and an ITO current spreader 610. Above the ITO current spreader 610, a layer of silicon oxide 692 is deposited, patterned, etched and filled with a metal 690 (e.g., tungsten) which is then CMPed. Examples of materials used to construct these layers, include, but are not limited to, doped AlInGaP for the N-type confinement layer 604 and P-type confinement layer 608, the multiple quantum well layer 606 could be of AlInGaP and GaInP and the optional reflector 609 could be a distributed Bragg Reflector. A double heterostructure configuration or single quantum well configuration could be used instead of a multiple quantum well configuration. Various other material types and configurations could be used for constructing the red LEDs for this process. Yet another wafer is constructed with a green LED. The green LED wafer 638 is constructed on a sapphire or SiC or bulk-GaN substrate 612 and includes a N-type confinement layer 614, a multiple quantum well (MQW) 616, a buffer layer 618, a P-type confinement layer 620, an optional reflector 621 and an ITO current spreader 622. Above the ITO current spreader 622, a layer of silicon oxide 696 is deposited, patterned, etched and filled with a metal 694 (e.g., tungsten) which is then CMPed. Yet another wafer is constructed with a blue LED. The blue LED wafer 640 is constructed on a sapphire or SiC or bulk-GaN substrate 624 and includes a N-type confinement layer 626, a multiple quantum well (MQW) 628, a buffer layer 630, a P-type confinement layer 632, an optional reflector 633 and an ITO current spreader 634. Above the ITO current spreader 634, a layer of silicon dioxide 698 is deposited. Examples of materials used to construct these blue and green LED layers, include, but are not limited to, doped GaN for the N-type and P-type confinement layers 614, 620, 626 and 632, AlGaN for the buffer layers 630 and 618 and InGaN/GaN for the multiple quantum wells 616 and 628. The optional reflectors 621 and 633 could be distributed Bragg Reflectors or some other type of reflectors. Various other material types and configurations could be used for constructing blue and green LEDs for this process.

Step (B) is illustrated in FIG. 6B. The blue LED wafer 640 from FIG. 6A is used for this step. Various elements in FIG. 6B such as 624, 626, 628, 630, 632, 633, 698, and 634 have been previously described. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines 642. Alternately, helium could be used for this step.

Step (C) is illustrated in FIG. 6C. A glass substrate 646 is taken and a silicon dioxide layer 688 is deposited atop it.

Step (D) is illustrated in FIG. 6D. The wafer shown in FIG. 6B is flipped and bonded atop the wafer shown in FIG. 6C using oxide-oxide bonding. Various elements in FIG. 6D such as 624, 626, 628, 630, 632, 633, 698, 642, 646, 688, and 634 have been previously described. The oxide layer 688 is essentially bonded to the oxide layer 698 using an oxide-to-oxide bonding process.

Step (E) is illustrated in FIG. 6E. Various elements in FIG. 6E such as 628, 630, 632, 633, 698, 646, 688, and 634 have been previously described. An ion-cut process is conducted to cleave the structure shown in FIG. 6D at the hydrogen implant plane 642. This ion-cut process may be preferably using a mechanical cleave. An anneal process could be utilized for the cleave as well. After the cleave, a chemical mechanical polish (CMP) process is conducted to planarize the surface. The N-type confinement layer present after this cleave and CMP process is indicated as 627.

Step (F) is illustrated in FIG. 6F. Various elements in FIG. 6F such as 628, 630, 632, 633, 698, 646, 688, 627, and 634 have been previously described. An ITO layer 648 is deposited atop the N-type confinement layer 627. Above the ITO layer

648, a layer of silicon oxide 686 is deposited, patterned, etched and filled with a metal 684 (e.g., tungsten) which is then CMPed.

Step (G) is illustrated in FIG. 6G. The green LED wafer 638 shown in Step (A) is used for this step. Various elements in FIG. 6G such as 612, 614, 616, 618, 620, 621, 696, 694, and 622 have been described previously. Hydrogen is implanted into the wafer at a certain depth indicated by dotted lines 650. Alternatively, helium could be used for this step.

Step (H) is illustrated in FIG. 6H. The structure shown in FIG. 6G is flipped and bonded atop the structure shown in FIG. 6F using oxide-oxide bonding. The metal regions 694 and 684 on the bonded wafers are aligned to each other. Various elements in FIG. 6H such as 628, 630, 632, 633, 698, 646, 688, 627, 634, 648, 686, 684, 612, 614, 616, 618, 620, 621, 696, 694, 650, and 622 have been described previously.

Step (I) is illustrated in FIG. 6I. The structure shown in FIG. 6H is cleaved at the hydrogen plane indicated by 650. This cleave process may be preferably done with a mechanical force. Alternatively, an anneal could be used. A CMP process is conducted to planarize the surface. Various elements in FIG. 6I such as 628, 630, 632, 633, 698, 646, 688, 627, 634, 648, 686, 684, 616, 618, 620, 621, 696, 694, and 622 have been described previously. The N-type confinement layer present after this cleave and CMP process is indicated as 615.

Step (J) is illustrated in FIG. 6J. An ITO layer 652 is deposited atop the structure shown in FIG. 6I. Above the ITO layer 652, a layer of silicon oxide 682 is deposited, patterned, etched and filled with a metal 680 (e.g., tungsten) which is then CMPed. Various elements in FIG. 6J such as 628, 630, 632, 633, 698, 646, 688, 627, 634, 648, 686, 684, 616, 618, 620, 621, 696, 694, 615, and 622 have been described previously.

Step (K) is illustrated in FIG. 6K. Using procedures similar to Step (G)-Step (J), the red LED layer is transferred atop the structure shown in FIG. 6J. The N-type confinement layer after ion-cut is indicated by 605. An ITO layer 656 is deposited atop the N-type confinement layer 605. Various elements in FIG. 6K such as 628, 630, 632, 633, 698, 646, 688, 627, 634, 648, 686, 684, 616, 618, 620, 621, 696, 694, 615, 690, 692, 610, 609, 608, 606, and 622 have been described previously.

Step (L) is illustrated in FIG. 6L. Using flip-chip packaging procedures similar to those described in FIG. 4A-FIG. 4S, the RGB LED stack shown in FIG. 6K is attached to a silicon sub-mount 668. 658 indicates a reflecting material, 664 is a nickel layer, 666 represents solder bumps, 670 is an aluminum via, and 672 is either an oxide layer or an air gap. Various elements in FIG. 6K such as 628, 630, 632, 633, 698, 646, 688, 627, 634, 648, 686, 684, 616, 618, 620, 621, 696, 694, 615, 690, 692, 610, 609, 608, 606, 605, 656, and 622 have been described previously. The configuration of optional reflectors 633, 621 and 609 determines light output coming from the LED. A preferred embodiment of this invention may not have a reflector 633, but may have the reflector 621 (reflecting only the blue light produced by multiple quantum well 628) and the reflector 609 (reflecting only the green light produced by multiple quantum well 616). In the process described in FIG. 6A-FIG. 6L, the original substrates in FIG. 6A, namely 602, 612, and 624, can be re-used after ion-cut. This may make the process more cost-effective.

FIGS. 7A-L illustrate an embodiment of this invention, where stacked RGB LEDs are formed with laser lift-off, substrate etch, flip-chip packaging and conductive oxide bonding. Essentially, smart layer transfer techniques are used. This process could include several steps that occur in a sequence from Step (A) to Step (M). Many of the steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A): This is illustrated using FIG. 7A. A red LED wafer 736 is constructed on a GaAs substrate 702 and includes a N-type confinement layer 704, a multiple quantum well (MQW) 706, a P-type confinement layer 708, an optional reflector 709 and an ITO current spreader 710. Examples of materials used to construct these layers, include, but are not limited to, doped AlInGaP for the N-type confinement layer 704 and P-type confinement layer 708, the multiple quantum well layer 706 could be of AlInGaP and GaInP and the optional reflector 409 could be a distributed Bragg Reflector. A double heterostructure configuration or single quantum well configuration could be used instead of a multiple quantum well configuration. Various other material types and configurations could be used for constructing the red LEDs for this process. Yet another wafer is constructed with a green LED. The green LED wafer 738 is constructed on a sapphire substrate 712 (or some other transparent substrate) and includes a N-type confinement layer 714, a multiple quantum well (MQW) 716, a buffer layer 718, a P-type confinement layer 720, an optional reflector 721 and an ITO current spreader 722. Yet another wafer is constructed with a blue LED. The blue LED wafer 740 is constructed on a sapphire substrate 724 (or some other transparent substrate) and includes a N-type confinement layer 726, a multiple quantum well (MQW) 728, a buffer layer 730, a P-type confinement layer 732, an optional reflector 733 and an ITO current spreader 734. Examples of materials used to construct these blue and green LED layers, include, but are not limited to, doped GaN for the N-type and P-type confinement layers 714, 720, 726 and 732, AlGaN for the buffer layers 730 and 718 and InGaN/GaN for the multiple quantum wells 716 and 728. The optional reflectors 721 and 733 could be distributed Bragg Reflectors or some other type of reflectors. Various other material types and configurations could be used for constructing blue and green LEDs for this process.

Step (B) is illustrated in FIG. 7B. A glass substrate 746 is taken and an ITO layer 744 is deposited atop it.

Step (C) is illustrated in FIG. 7C. The blue LED wafer 740 shown in FIG. 7A is flipped and bonded atop the wafer shown in FIG. 7B using ITO-ITO bonding. Various elements in FIG. 7C such as 724, 726, 728, 730, 732, 733, 734, 746, and 744 have been previously described. The ITO layer 744 is essentially bonded to the ITO layer 734 using an oxide-to-oxide bonding process.

Step (D) is illustrated in FIG. 7D. A laser is used to shine radiation through the sapphire substrate 724 of FIG. 7C and a laser lift-off process is conducted. The sapphire substrate 724 of FIG. 7C is removed with the laser lift-off process. Further details of the laser lift-off process are described in U.S. Pat. No. 6,071,795 by Nathan W. Cheung, Timothy D. Sands and William S. Wong ("Cheung"). A CMP process is conducted to planarize the surface of the N confinement layer 727 after laser lift-off of the sapphire substrate. Various elements in FIG. 7D such as 728, 730, 732, 733, 734, 746, and 744 have been previously described.

Step (E) is illustrated in FIG. 7E. Various elements in FIG. 7E such as 728, 730, 732, 733, 734, 746, 727, and 744 have been previously described. An ITO layer 748 is deposited atop the N confinement layer 727.

Step (F) is illustrated in FIG. **7**F. The green LED wafer **738** is flipped and bonded atop the structure shown in FIG. **7**E using ITO-ITO bonding of layers **722** and **748**. Various elements in FIG. **7**F such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, **714**, **712** and **744** have been previously described.

Step (G) is illustrated in FIG. **7**G. A laser is used to shine radiation through the sapphire substrate **712** of FIG. **7**F and a laser lift-off process is conducted. The sapphire substrate **712** of FIG. **7**F is removed with the laser lift-off process. A CMP process is conducted to planarize the surface of the N-type confinement layer **715** after laser lift-off of the sapphire substrate. Various elements in FIG. **7**G such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, and **744** have been previously described.

Step (H) is illustrated in FIG. **7**H. An ITO layer **752** is deposited atop the N-type confinement layer **715**. Various elements in FIG. **7**H such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, **715**, and **744** have been previously described.

Step (I) is illustrated in FIG. **7**I. The red LED wafer **736** from FIG. **7**A is flipped and bonded atop the structure shown in FIG. **7**H using ITO-ITO bonding of layers **710** and **752**. Various elements in FIG. **7**I such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, **715**, **752**, **710**, **709**, **708**, **706**, **704**, **702**, and **744** have been previously described.

Step (J) is illustrated in FIG. **7**J. The GaAs substrate **702** from FIG. **7**I is removed using etch and/or CMP. Following this etch and/or CMP process, the N-type confinement layer **704** of FIG. **7**I is planarized using CMP to form the N-type confinement layer **705**. Various elements in FIG. **7**J such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, **715**, **752**, **710**, **709**, **708**, **706**, and **744** have been previously described.

Step (K) is illustrated in FIG. **7**K. An ITO layer **756** is deposited atop the N confinement layer **705** of FIG. **7**J. Various elements in FIG. **7**K such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, **715**, **752**, **710**, **709**, **708**, **706**, **705**, and **744** have been previously described.

Step (L) is illustrated in FIG. **7**L. Using flip-chip packaging procedures similar to those described in FIG. **4**A-FIG. **4**S, the RGB LED stack shown in FIG. **7**K is attached to a silicon sub-mount **768**. **758** indicates a reflecting material, **764** is a nickel layer, **766** represents solder bumps, **762** is an aluminum via, and **772** is either an oxide layer or an air gap. Various elements in FIG. **7**L such as **728**, **730**, **732**, **733**, **734**, **746**, **727**, **748**, **722**, **721**, **720**, **718**, **716**, **715**, **752**, **710**, **709**, **708**, **706**, **705**, and **756** have been described previously. The configuration of optional reflectors **733**, **721** and **709** determines light output coming from the LED. The preferred embodiment of this invention may not have a reflector **733**, but may have the reflector **721** (reflecting only the blue light produced by multiple quantum well **728**) and the reflector **709** (reflecting only the green light produced by multiple quantum well **716**).

FIGS. **8**A-B show an embodiment of this invention, where stacked RGB LEDs are formed from a wafer having red LED layers and another wafer having both green and blue LED layers. Therefore, a smart layer transfer process is used to form the stacked RGB LED. FIG. **8**A shows that a red LED wafer **836** and another wafer called a blue-green LED wafer **836** are used. The red LED wafer **836** is constructed on a GaAs substrate **802** and includes a N-type confinement layer **804**, a multiple quantum well (MQW) **806**, a P-type confinement layer **808**, an optional reflector **809** and an ITO current spreader **810**. Examples of materials used to construct these layers, include, but are not limited to, doped AlInGaP for the N-type confinement layer **804** and P-type confinement layer **808**, the multiple quantum well layer **806** could be of AlInGaP and GaInP and the optional reflector **809** could be a distributed Bragg Reflector. A double heterostructure configuration or single quantum well configuration could be used instead of a multiple quantum well configuration. Various other material types and configurations could be used for constructing the red LEDs for this process. The blue-green LED wafer **838** is constructed on a sapphire or bulk GaN or SiC substrate **812** (or some other transparent substrate) and includes a N-type confinement layer **814**, a green multiple quantum well (MQW) **816**, a blue multiple quantum well **817**, a buffer layer **818**, a P-type confinement layer **820**, an optional reflector **821**, and an ITO current spreader **822**. Examples of materials used to construct the blue-green LED wafers, include, but are not limited to, doped GaN for the N-type and P-type confinement layers **814**, **820**, AlGaN for the buffer layer **818** and InGaN/GaN for the multiple quantum wells **816** and **817**. The optional reflector **821** could be a distributed Bragg Reflector or some other type of reflector. The optional reflector **821** could alternatively be built between the N-type confinement layer **814** or below it, and this is valid for all LEDs discussed in the patent application. Various other material types and configurations could be used for constructing blue-green LED wafers for this process. Using smart layer transfer procedures similar to those shown in FIG. **4**-FIG. **7**, the stacked RGB LED structure shown in FIG. **8**B is constructed. Various elements in FIG. **8**B such as **806**, **808**, **809**, **810**, **816**, **817**, **818**, **820**, **821**, and **822** have been described previously. **846** is a glass substrate, **844** is an ITO layer, **815** is a N-type confinement layer for a blue-green LED, **852** is an ITO layer, **805** is a N-type confinement layer for a red LED, **856** is an ITO layer, **858** is a reflecting material such as, for example, silver or aluminum, **864** is a nickel layer, **866** is a solder layer, **862** is a contact layer constructed of aluminum or some other metal, **860** may be preferably an air gap but could be an oxide layer and **868** is a silicon sub-mount. The configuration of optional reflectors **821** and **809** determines light produced by the LED. For the configuration shown in FIG. **8**B, the preferred embodiment may not have the optional reflector **821** and may have the optional reflector **809** reflecting light produced by the blue and green quantum wells **816** and **817**.

FIG. **9** illustrates an embodiment of this invention, where stacked RGB LEDs are formed with control and driver circuits for the LED built on the silicon sub-mount. Procedures similar to those described in FIG. **4**-FIG. **7** are utilized for constructing and packaging the LED. Control and driver circuits are integrated on the silicon sub-mount **968** and can be used for controlling and driving the stacked RGB LED. **946** is a glass substrate, **944** and **934** are ITO layers, **933** is an optional reflector, **932** is a P-type confinement layer for a blue LED, **930** is a buffer layer for a blue LED, **928** is a blue multiple quantum well, **927** is a N-type confinement layer for a blue LED, **948** and **922** are ITO layers, **921** is an optional reflector, **920** is a P-type confinement layer for a green LED, **918** is a buffer layer for a green LED, **916** is a multiple quantum well for a green LED, **915** is a N-type confinement layer for a green LED, **952** and **910** are ITO layers, **909** is a reflector, **908** is a P-type confinement layer for a red LED, **906** is a red multiple quantum well, **905** is a N-type confinement layer for a red LED, **956** is an ITO layer, **958** is a reflecting layer such as aluminum or silver, **962** is a metal via constructed, for example, out of aluminum, **960** is an air-gap or an oxide layer, **964** is a nickel layer, and **966** is a solder bump.

FIG. **10** illustrates an embodiment of this invention, where stacked RGB LEDs are formed with control and driver circuits as well as image sensors for the LED built on the silicon sub-mount **1068**. Image sensors essentially monitor the light coming out of the LED and tune the voltage and current given by control and driver circuits such that light output of the LED is the right color and intensity. **1046** is a glass substrate, **1044** and **1034** are ITO layers, **1033** is an optional reflector, **1032** is a P-type confinement layer for a blue LED, **1030** is a buffer layer for a blue LED, **1028** is a blue multiple quantum well, **1027** is a N-type confinement layer for a blue LED, **1048** and **1022** are ITO layers, **1021** is an optional reflector, **1020** is a P-type confinement layer for a green LED, **1018** is a buffer layer for a green LED, **1016** is a multiple quantum well for a green LED, **1015** is a N-type confinement layer for a green LED, **1052** and **1010** are ITO layers, **1009** is a reflector, **1008** is a P-type confinement layer for a red LED, **1006** is a red multiple quantum well, **1005** is a N-type confinement layer for a red LED, **1056** is an ITO layer, **1058** is a reflecting layer such as aluminum or silver, **1062** is a metal via constructed for example out of aluminum, an air-gap or an oxide layer between silicon sub-mount **1068** and reflecting layer **1058**, **1064** is a nickel layer and **1066** is a solder bump. The via hole **1074** helps transfer light produced by the blue multiple quantum well **1028** reach an image sensor on the silicon sub-mount **1068**. The via hole **1072** helps transfer light produced by the green multiple quantum well **1016** to an image sensor on the silicon sub-mount **1068**. The via hole **1070** helps transfer light produced by the red multiple quantum well **1006** reach an image sensor on the silicon sub-mount **1068**. By sampling the light produced by each of the quantum wells on the LED, voltage and current drive levels to different terminals of the LED can be determined. Color tunability, temperature compensation, better color stability, and many other features can be obtained with this scheme. Furthermore, circuits to communicate wirelessly with the LED can be constructed on the silicon sub-mount. Light output of the LED can be modulated by a signal from the user delivered wirelessly to the light.

While three LED layers, namely, red, green, and blue, are shown as stacked in various embodiments of this invention, it will be clear to one skilled in the art based on the present disclosure that more than three LED layers can also be stacked. For example, red, green, blue and yellow LED layers can be stacked.

The embodiments of this invention described in FIG. **4**-FIG. **10** share a few common features. They have multiple stacked (or overlying) layers, they are constructed using smart layer transfer techniques and at least one of the stacked layers has a thickness less than 50 microns. When cleave is done using ion-cut, substrate layers that are removed using cleave can be reused after a process flow that often includes a CMP.

FIGS. **11**A-F show a prior art illustration of phosphor-coated LEDs (pcLEDs) constructed with ion-cut processes. The process begins in FIG. **11**A with a bulk-GaN substrate **1102**, and an oxide layer **1104** is deposited atop it. The oxide layer **1104** is an oxide compatible with GaN. FIG. **11**B depicts hydrogen being implanted into the structure shown in FIG. **11**A at a certain depth (for ion-cut purposes). **1102** and **1104** have been described previously with respect to FIG. **11**A. Dotted lines **1106** indicate the plane of hydrogen ions. Alternatively, helium can be implanted instead of hydrogen or hydrogen and helium can be co-implanted. FIG. **11**C shows a silicon wafer **1108** with an oxide layer **1110** atop it. The structure shown in FIG. **11**B is flipped and bonded atop the structure shown in FIG. **11**C using oxide-to-oxide bonding of layers **1104** and **1110**. This is depicted in FIG. **11**D. **1108**, **1110** and **1106** have been described previously. FIG. **11**E shows the next step in the process. Using an anneal, a cleave is conducted at the plane of hydrogen atoms **1106** shown in FIG. **11**D, and a CMP is done to form GaN layer **1112**. **1104**, **1110** and **1108** have been described previously. FIG. **11**F shows the following step in the process. A blue LED **1114** is grown epitaxially above the GaN layer **1112**. **1104**, **1108** and **1110** have been described previously. A phosphor layer can be coated atop the blue LED **1114** to form a white phosphor coated LED.

There may be some severe challenges with the prior art process shown in FIGS. **11**A-F. The thermal expansion coefficients for GaN layers **1112** in FIG. **11**F are very different from that for silicon layers **1108**. This difference can cause cracks and defects while growing the blue LED layer **1114** at high temperatures (>600° C.), which usually occurs. These cracks and defects, in turn, cause bad efficiency and can in turn cause the phosphor coated LED process in FIG. **11**A-F to be difficult to manufacture. Furthermore, an anneal (typically >400° C.) is typically used in FIG. **11**E to cleave the bulk GaN layers. This can again cause issues with mismatch of thermal expansion co-efficients and cause cracking and defects.

FIGS. **12**A-F describe an embodiment of this invention, where phosphor coated LEDs are formed with an ion-cut process (i.e. a smart layer transfer process). It minimizes the problem with mismatch of thermal expansion co-efficients that is inherent to the process described in FIGS. **11**A-F. This process could include several steps as described in the following sequence:

Step (A): FIG. **12**A illustrates this step. A blue LED wafer is constructed on a bulk-GaN substrate **1216**. For discussions within this document, the bulk-GaN substrate could be semi-polar or non-polar or polar. The blue LED wafer includes a N-type confinement layer **1214**, a multiple quantum well (MQW) **1212**, a buffer layer **1210**, a P-type confinement layer **1208**, an optional reflector **1204** and an ITO current spreader **1206**. Examples of materials used to construct these blue LED layers, include, but are not limited to, doped GaN for the N-type and P-type confinement layers **1214** and **1208**, AlGaN for the buffer layer **1210** and InGaN/GaN for the multiple quantum wells **1212**. The optional reflector **1204** could be distributed Bragg Reflector, an Aluminum or silver layer or some other type of reflectors. A silicon dioxide layer **1202** is deposited atop the optional reflector **1204**.

Step (B): FIG. **12**B illustrates this step. The blue LED wafer described in FIG. **12**A has hydrogen implanted into it at a certain depth. The dotted lines **1218** depict the hydrogen implant. Alternatively, helium can be implanted. Various elements in FIG. **12**B such as **1216**, **1214**, **1212**, **1210**, **1208**, **1206**, **1204**, and **1202** have been described previously.

Step (C): FIG. **12**C illustrates this step. A wafer **1220**, preferably of silicon, having the same wafer size as the structure in FIG. **12**B is taken and an oxide layer **1222** is grown or deposited atop it.

Step (D): FIG. **12**D illustrates this step. The structure shown in FIG. **12**B is flipped and bonded atop the structure shown in FIG. **12**C using oxide-to-oxide bonding of layers **1202** and **1222**. Various elements in FIG. **12**D such as **1216**, **1214**, **1212**, **1210**, **1208**, **1206**, **1204**, **1220**, **1222**, **1218** and **1202** have been described previously.

Step (E): FIG. **12**E illustrates this step. The structure shown in FIG. **12**D is cleaved at its hydrogen plane **1218**. A mechanical cleave may be preferably used for this process. However, an anneal could be used as well. The mechanical cleave process typically happens at room temperatures, and therefore can avoid issues with thermal expansion co-efficients mismatch. After cleave, the wafer is planarized and the N-type confinement layer **1215** is formed. Various elements in FIG. **12**E such as **1212**, **1210**, **1208**, **1206**, **1204**, **1220**, **1222**, and **1202** have been described previously. The bulk GaN substrate **1216** from FIG. **12**D that has been cleaved away can be reused. This may be attractive from a cost perspective, since bulk GaN substrates are quite costly.

Step (F): This is illustrated in FIG. **12**F. An ITO layer **1224** is deposited atop the structure shown in FIG. **12**E. Various elements in FIG. **12**F such as **1212**, **1210**, **1208**, **1206**, **1204**, **1220**, **1222**, **1215**, **1224**, and **1202** have been described previously.

A phosphor coating can be applied over the structure shown in FIG. **12**F to produce a phosphor-coated LED. The advantage of the process shown in FIG. **12**A-F over the process shown in FIG. **11**A-F may include low process temperatures, even less than 250° C. Therefore, issues with thermal expansion co-efficients mismatch are substantially mitigated. While the description in FIG. **12**A-F is for a LED, many other devices, such as, for example, laser diodes, high power transistors, high frequencies transistors, special transmitter circuits and many other devices can be constructed, according to a similar description, with bulk-GaN.

In the description of FIG. **12**A-F, silicon is described as a preferred material for the substrate **1220**. Silicon has a co-efficient of thermal expansion of about 2.6 ppm/° C., while bulk-GaN, which is the substrate **1216** on which the LED is epitaxially grown, has a co-efficient of thermal expansion of 5.6 ppm/° C. In an alternate embodiment of this invention, the substrate **1220** used in FIG. **12**A-F could be constructed of a material that has a co-efficient of thermal expansion (CTE) fairly close to bulk-GaN. Preferably, the CTE of the substrate **1220** could be any value in between (the CTE of bulk GaN −2 ppm/° C.) and (the CTE of bulk GaN+2 ppm/° C.). Examples of materials that could be used for the substrate **1220** could include, but are not limited to, Germanium, that has a CTE of 5.8 ppm/° C., and various ceramic materials. Having CTE for the substrate **1220** close to bulk-GaN prevents defects and cracks being formed due to issues with mismatch of CTE, even if higher temperature processing (>250° C.) is used.

In an alternative embodiment of this invention, the flow in FIG. **11**A-F can be used with the substrate **1108** having a CTE fairly close to the CTE of bulk GaN. Preferably, the CTE of the substrate **1108** could be any value in between (the CTE of bulk GaN−2 ppm/° C.) and (the CTE of bulk GaN+2 ppm/° C.). Examples of materials that could be used for the substrate **1108** could include, but are not limited to, Germanium, that has a CTE of 5.8 ppm/° C., and various ceramic materials.

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Layer transfer technology can also be advantageously utilized for constructing image sensors. Image sensors typically include photodetectors on each pixel to convert light energy to electrical signals. These electrical signals are sensed, amplified and stored as digital signals using transistor circuits.

FIG. **13** shows prior art where through-silicon via (TSV) technology is utilized to connect photodetectors **1302** on one layer (tier) of silicon to transistor read-out circuits **1304** on another layer (tier) of silicon. Unfortunately, pixel sizes in today's image sensors are 1.1 μm or so. It is difficult to get through-silicon vias with size <1 μm due to alignment problems, leading to a diminished ability to utilize through-silicon via technology for future image sensors. In FIG. **13**, essentially, transistors can be made for read-out circuits in one wafer, photodetectors can be made on another wafer, and then these wafers can be bonded together with connections made with through-silicon vias.

FIGS. **14**-**21** describe some embodiments of this invention, where photodetector and read-out circuits are stacked monolithically with layer transfer. FIG. **14** shows two configurations for stacking photodetectors and read-out circuits. In one configuration, denoted as **1402**, a photodetector layer **1406** may be formed above read-out circuit layer **1408** with connections **1404** between these two layers. In another configuration, denoted as **1410**, photodetectors **1412** may have read-out circuits **1414** formed above them, with connections **1416** between these two layers.

FIGS. **15**A-H describe an embodiment of this invention, where an image sensor includes a photodetector layer formed atop a read-out circuit layer using layer transfer. In this document, the photodetector layer is denoted as a p-n junction layer. However, any type of photodetector layer, such as a pin layer or some other type of photodetector can be used. The thickness of the photodetector layer is typically less than 5 μm. The process of forming the image sensor could include several steps that occur in a sequence from Step (A) to Step (H). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **15**A. A silicon wafer **1502** may be taken and a n+ Silicon layer **1504** may be formed by ion implantion. Following this, n layer **1506**, p layer **1508** and p+ layer **1510** may be formed epitaxially. It will be appreciated by one skilled in the art based on the present disclosure that there are various other procedures to form the structure shown in FIG. **15**A. An anneal may then be performed to activate dopants in the various layers.

Step (B) is illustrated in FIG. **15**B. Various elements in FIG. **15**B such as **1502**, **1504**, **1506**, **1508** and **1510** have been described previously. Using lithography and etch, a via may be etched into the structure shown in FIG. **15**A, then may be filled with oxide and then polished with CMP. The regions formed are the oxide filled via **1512** and the oxide layer **1514**. The oxide filled via **1512** may also be referred to as an oxide via or an oxide window region or oxide aperture. A cross-section of the structure is indicated by **1598** and a top view is indicated by **1596**. **1516** indicates alignment marks and the oxide filled via **1512** may be formed in place of some of the alignment marks printed on the wafer.

Step (C) is illustrated in FIG. **15**C. Various elements in FIG. **15**C such as **1502**, **1504**, **1506**, **1508**, **1510**, **1512**, **1514**, and **1516** have been described previously. Hydrogen may be implanted into the structure indicated in FIG. **15**B at a certain depth indicated by dotted lines **1518** of FIG. **15**C. Alternatively, Helium can be used as the implanted species. A cross-sectional view **1594** and a top view **1592** are shown.

Step (D) is illustrated in FIG. **15**D. A silicon wafer **1520** with read-out circuits (which includes wiring) processed on it is taken, and an oxide layer **1522** may be deposited above it.

Step (E) is illustrated in FIG. **15**E. The structure shown in FIG. **15**C is flipped and bonded to the structure shown in FIG. **15**D using oxide-to-oxide bonding of oxide layers **1514** and **1522**. During this bonding procedure, alignment may be done such that oxide vias **1512** (shown in the top view **1526** of the photodetector wafer) are above alignment marks (such as **1530**) on the top view **1528** of the read-out circuit wafer. A cross-sectional view of the structure is shown with **1524**.

Various elements in FIG. **15**E such as **1502**, **1504**, **1506**, **1508**, **1510**, **1512**, **1514**, **1516**, **1518**, **1520**, and **1522** have been described previously.

Step (F) is illustrated in FIG. **15**F. The structure shown in FIG. **15**E may be cleaved at its hydrogen plane **1518** preferably using a mechanical process. Alternatively, an anneal could be used for this purpose. A CMP process may be then done to planarize the surface resulting in a final n+ silicon layer indicated as **1534**. **1525** depicts a cross-sectional view of the structure after the cleave and CMP process. Various elements in FIG. **15**F such as **1506**, **1508**, **1510**, **1512**, **1514**, **1516**, **1520**, **1526**, **1530**, **1528**, **1530** and **1522** have been described previously.

Step (G) is illustrated using FIG. **15**G. Various elements in FIG. **15**G such as **1506**, **1508**, **1510**, **1512**, **1514**, **1516**, **1520**, **1526**, **1530**, **1528**, **1530**, **1534** and **1522** have been described previously. An oxide layer **1540** may be deposited. Connections between the photodetector and read-out circuit wafers may be formed with metal **1538** and an insulator covering **1536**. These connections may be formed well aligned to the read-out circuit layer **1520** by aligning to alignment marks **1530** on the read-out circuit layer **1520** through oxide vias **1512**. **1527** depicts a cross-sectional view of the structure.

Step (H) is illustrated in FIG. **15**H. Connections are made to the terminals of the photodetector and are indicated as **1542** and **1544**. Various elements of FIG. **15**H such as **1520**, **1522**, **1512**, **1514**, **1510**, **1508**, **1506**, **1534**, **1536**, **1538**, **1540**, **1542**, and **1544** have been described previously. Contacts and interconnects for connecting terminals of the photodetector to read-out circuits may then be done, following which a packaging process is conducted.

The thinner the transferred layer, the smaller the through layer via (TLV) diameter obtainable, due to the potential limitations of manufacturable via aspect ratios. Thus, the transferred layer may be, for example, less than about 2 microns thick, less than about 1 micron thick, less than about 0.4 microns thick, less than about 200 nm thick, or less than about 100 nm thick. The vertical connections, or Through Layer Via (TLV) diameter may be less than about 400 nm, less than about 200 nm, less than about 80 nm, less than about 40 nm, or less than about 20 nm. The thickness of the layer or layers transferred according to some embodiments of the present invention may be designed as such to match and enable the best obtainable lithographic resolution capability of the manufacturing process employed to create the through layer vias or any other structures on the transferred layer or layers.

In many of the embodiments of the invention, the layer or layers transferred may be of a crystalline material, for example, mono-crystalline silicon, and after layer transfer, further processing, such as, for example, plasma/RIE or wet etching, may be done on the layer or layers that may create islands or mesas of the transferred layer or layers of crystalline material, for example, mono-crystalline silicon, the crystal orientation of which has not changed. Thus, a mono-crystalline layer or layers of a certain specific crystal orientation may be layer transferred and then processed whereby the resultant islands or mesas of mono-crystalline silicon have the same crystal specific orientation as the layer or layers before the processing. After this processing, the resultant islands or mesas of crystalline material, for example, mono-crystalline silicon, may be still referred to herein as a layer, for example, mono-crystalline layer, layer of mono-crystalline silicon, and so on

FIGS. **15**A-G show a process where oxide vias may be used to look through photodetector layers to observe alignment marks on the read-out circuit wafer below it. However, if the thickness of the silicon on the photodetector layer is <100-400 nm, the silicon wafer is thin enough that one can look through it without requiring oxide vias. A process similar to FIG. **15**A-G where the silicon thickness for the photodetector is <100-400 nm represents another embodiment of this invention. In that embodiment, oxide vias may not be constructed and one could look right through the photodetector layer to observe alignment marks of the read-out circuit layer. This may help making well-aligned through-silicon connections between various layers.

As mentioned previously, FIGS. **15**A-G illustrate a process where oxide vias constructed before layer transfer are used to look through photodetector layers to observe alignment marks on the read-out circuit wafer below it. However, an alternative embodiment of this invention may involve constructing oxide vias after layer transfer. Essentially, after layer transfer of structures without oxide vias, oxide vias whose diameters are larger than the maximum misalignment of the bonding/alignment scheme are formed. This order of sequences may enable observation of alignment marks on the bottom read-out circuit wafer by looking through the photodetector wafer.

While Silicon has been suggested as the material for the photodetector layer of FIG. **15**A-G, Germanium could be used in an alternative embodiment. The advantage of Germanium is that it is sensitive to infra-red wavelengths as well. However, Germanium also suffers from high dark current.

While FIG. **15**A-G described a single p-n junction as the photodetector, it will be obvious to one skilled in the art based on the present disclosure that multiple p-n junctions can be formed one on top of each other, as described in "Color Separation in an Active Pixel Cell Imaging Array Using a Triple-Well Structure," U.S. Pat. No. 5,965,875, 1999 by R. Merrill and in "Trends in CMOS Image Sensor Technology and Design," International Electron Devices Meeting Digest of Technical Papers, 2002 by A. El-Gamal. This concept relies on the fact that different wavelengths of light penetrate to different thicknesses of silicon, as described in FIG. **16**. It can be observed in FIG. **16** that near the surface 400 nm wavelength light has much higher absorption per unit depth than 450 nm-650 nm wavelength light. On the other hand, at a depth of 0.5 μm, 500 nm light has a higher absorption per unit depth than 400 nm light. An advantage of this approach is that one does not require separate filters (and area) for green, red and blue light; all these different colors/wavelengths of light can be detected with different p-n junctions stacked atop each other. So, the net area required for detecting three different colors of light is reduced, leading to an improvement of resolution.

FIGS. **17**A-B illustrate an embodiment of this invention, where red, green, and blue photodetectors are stacked monolithically atop read-out circuits using ion-cut technology (for an image sensor). Therefore, a smart layer transfer technique is utilized. FIG. **17**A shows the first step for constructing this image sensor. **1724** shows a cross-sectional view of **1708**, a silicon wafer with read-out circuits constructed on it, above which an oxide layer **1710** is deposited. **1726** shows the cross-sectional view of another wafer which may include silicon substrate **1712**, a p+ Silicon layer **1714**, a p Silicon layer **1716**, a n Silicon layer **1718**, a n+ Silicon layer **1720**, and an oxide layer **1722**. These layers may be formed using procedures similar to those described in FIG. **15**A-G. An anneal may then be performed to activate dopants in various layers. Hydrogen may be implanted in the wafer at a certain depth depicted by **1798**, shown as dashed line. FIG. **17**B shows the structure of the image sensor before contact formation. Three layers of p+pnn+ silicon (each corresponding to a color band and similar to the one depicted in **1726** in FIG. **17**A) are layer transferred sequentially atop the silicon wafer with read-out circuits (depicted by **1724** in FIG. **17**A). Three different layer transfer steps may be used for this purpose. Procedures for layer transfer and alignment for forming the image sensor in FIG. **17**B are similar to procedures used for constructing the image sensor shown in FIGS. **15**A-G. Each of the three layers of p+pnn+ silicon senses a different wavelength of light. For example, blue light is detected by blue photodetector **1702**, green light is detected by green photodetector **1704**, and red light is detected by red photodetector **1706**. Contacts, metallization, packaging and other steps are done to the structure shown in FIG. **17**B to form an image sensor. The oxides **1730** and **1732** could be either transparent conducting oxides or silicon dioxide. Use of transparent conducting oxides could allow fewer contacts to be formed.

FIG. **18**A-B show another embodiment of this invention, where red, green and blue photodetectors are stacked monolithically atop read-out circuits using ion-cut technology (for an image sensor) using a different configuration. Therefore, a smart layer transfer technique is utilized. FIG. **18**A shows the first step for constructing this image sensor. **1824** shows a cross-section of **1808**, a silicon wafer with read-out circuits constructed on it, above which an oxide layer **1810** is deposited. **1826** shows the cross-sectional view of another wafer which has silicon substrate **1812**, a p+ Silicon layer **1814**, a p Silicon layer **1816**, a n Silicon layer **1818**, a p Silicon layer **1820**, a n Silicon layer **1822**, a n+ Silicon layer **1828** and an oxide layer **1830**. These layers may be formed using procedures similar to those described in FIG. **15**A-G. An anneal may then be performed to activate dopants in various layers. Hydrogen may implanted in the wafer at a certain depth depicted by **1898**, shown as dashed line. FIG. **18**B shows the structure of the image sensor before contact formation. A layer of p+pnpnn+ (similar to the one depicted in **1826** in FIG. **18**A) is layer transferred sequentially atop the silicon wafer with read-out circuits (depicted by **1824** in FIG. **18**A). Procedures for layer transfer and alignment for forming the image sensor in FIG. **18**B are similar to procedures used for constructing the image sensor shown in FIG. **15**A-G. Contacts, metallization, packaging and other steps are done to the structure shown in FIG. **18**B to form an image sensor. Three different pn junctions, denoted by **1802**, **1804** and **1806** may be formed in the image sensor to detect different wavelengths of light.

FIGS. **19**A-B show another embodiment of this invention, where an image sensor that can detect both visible and infrared light is depicted. Such image sensors could be useful for taking photographs in both day and night settings (without necessarily requiring a flash). This embodiment makes use of the fact that while silicon is not sensitive to infra-red light, other materials such as Germanium and Indium Gallium Arsenide are. A smart layer transfer technique is utilized for this embodiment. FIG. **19**A shows the first step for constructing this image sensor. **1902** shows a cross-sectional view of **1904**, a silicon wafer with read-out circuits constructed on it, above which an oxide layer **1906** is deposited. **1908** shows the cross-sectional view of another wafer which has silicon **1910**, a p+ Silicon layer **1912**, a p Silicon layer **1914**, a n Silicon layer **1916**, a n+ Silicon layer **1918** and an oxide layer **1720**. These layers may be formed using procedures similar to those described in FIGS. **15**A-G. An anneal may then be performed to activate dopants in various layers. Hydrogen may be implanted in the wafer at a certain depth depicted by **1998**, shown as dashed line. **1922** shows the cross-sectional view of another wafer which has a substrate **1924**, an optional buffer layer **1936**, a p+ Germanium layer **1926**, a p Germanium layer **1928**, a n Germanium layer **1930**, a n+ Germanium layer **1932** and an oxide layer **1934**. These layers may be formed using procedures similar to those described in FIGS. **15**A-G. An anneal may then be performed to activate dopants in various layers. Hydrogen may be implanted in the wafer at a certain depth depicted by **1996**, shown as dashed line. Examples of materials used for the structure **1922** may include a Germanium substrate for **1924**, no buffer layer and multiple Germanium layers. Alternatively, an Indium Phosphide substrate could be used for **1924** when the layers **1926**, **1924**, **1922** and **1920** are constructed of InGaAs instead of Germanium. FIG. **19**B shows the structure of this embodiment of the invention before contacts and metallization are constructed. The p+pnn+ Germanium layers of structure **1922** of FIG. **19**A are layer transferred atop the read-out circuit layer of structure **1902**. This is done using smart layer transfer procedures similar to those described in respect to FIG. **15**A-G. Following this, multiple p+pnn+ layers similar to those used in structure **1908** may be layer transferred atop the read-out circuit layer and Germanium photodetector layer (using three different layer transfer steps). This, again, is done using procedures similar to those described in FIGS. **15**A-G. The structure shown in FIG. **19**B therefore has a layer of read-out circuits **1904**, above which an infra-red photodetector **1944**, a red photodetector **1942**, a green photodetector **1940** and a blue photodetector **1938** are present. Procedures for layer transfer and alignment for forming the image sensor in FIG. **19**B are similar to procedures used for constructing the image sensor shown in FIG. **15**A-G. Each of the p+pnn+ layers senses a different wavelength of light. Contacts, metallization, packaging and other steps are done to the structure shown in FIG. **19**B to form an image sensor. The oxides **1946**, **1948**, and **1950** could be either transparent conducting oxides or silicon dioxide. Use of transparent conducting oxides could allow fewer contacts to be formed.

FIG. **20**A describes another embodiment of this invention, where polarization of incoming light can be detected. The p-n junction photodetector **2006** detects light that has passed through a wire grid polarizer **2004**. Details of wire grid polarizers are described in "Fabrication of a 50 nm half-pitch wire grid polarizer using nanoimprint lithography." Nanotechnology 16 (9): 1874-1877, 2005 by Ahn, S. W.; K. D. Lee, J. S. Kim, S. H. Kim, J. D. Park, S. H. Lee, P. W. Yoon. The wire grid polarizer **2004** absorbs one plane of polarization of the incident light, and may enable detection of other planes of polarization by the p-n junction photodetector **2006**. The p-n junction photodetector **2002** detects all planes of polarization for the incident light, while **2006** detects the planes of polarization that are not absorbed by the wire grid polarizer **2004**. One can thereby determine polarization information from incoming light by combining results from photodetectors **2002** and **2006**. The device described in FIG. **20**A can be fabricated by first constructing a silicon wafer with transistor circuits **2008**, following which the p-n junction photodetector **2006** can be constructed with the low-temperature layer transfer techniques described in FIG. **15**A-G. Following this construction of p-n junction photodetector **2006**, the wire grid polarizer **2004** may be constructed using standard integrated circuit metallization methods. The photodetector **2002** can then be constructed by another low-temperature layer transfer process as described in FIG. **15**A-G. One skilled in the art, based on the present disclosure, can appreciate that low-temperature layer transfer techniques are critical to build this device, since semiconductor layers in **2002** are built atop metallization layers required for the wire grid polarizer **2004**. Thickness of the photodetector layers **2002** and **2006** may be preferably less than 5 μm. An example with polarization detection where the photodetector has other pre-processed optical interaction layers (such as a wire grid polarizer) has been described herein. However, other devices for determining parameters of incoming light (such as phase) may be constructed with layer transfer techniques.

One of the common issues with taking photographs with image sensors is that in scenes with both bright and dark areas, while the exposure duration or shutter time could be set high enough to get enough photons in the dark areas to reduce noise, picture quality in bright areas degrades due to saturation of the photodetectors' characteristics. This issue is with the dynamic range of the image sensor, i.e. there is a tradeoff between picture quality in dark and bright areas. FIG. **20**B shows an embodiment of this invention, where higher dynamic range can be reached. According the embodiment of FIG. **20**B, two layers of photodetectors **2032** and **2040**, could be stacked atop a read-out circuit layer **2028**. **2026** is a schematic of the architecture. Connections **2030** run between the photodetector layers **2032** and **2040** and the read-out circuit layer **2028**. **2024** are reflective metal lines that block light from reaching part of the bottom photodetector layer **2032**. **2042** is a top view of the photodetector layer **2040**. Photodetectors **2036** could be present, with isolation regions **2038** between them. **2044** is a top view of the photodetector layer **2032** and the metal lines **2024**. Photodetectors **2048** are present, with isolation regions **2046** between them. A portion of the photodetectors **2048** can be seen to be blocked by metal lines **2024**. Brighter portions of an image can be captured with photodetectors **2048**, while darker portions of an image can be captured with photodetectors **2036**. The metal lines **2024** positioned in the stack may substantially reduce the number of photons (from brighter portions of the image) reaching the bottom photodetectors **2048**. This reduction in number of photons reaching the bottom photodetectors **2048** helps keep the dynamic range high. Read-out signals coming from both dark and bright portions of the photodetectors could be used to get the final picture from the image sensor.

FIG. **21** illustrates another embodiment of this invention where a read-out circuit layer **2104** is monolithically stacked above the photodetector layer **2102** at a temperature approximately less than 400° C. Connections **2106** are formed between these two layers. Procedures for stacking high-quality monocrystalline transistor circuits and wires at temperatures approximately less than 400° C. using layer transfer are described in pending U.S. patent application Ser. No. 12/901,890 by the inventors of this patent application, the content of which is incorporated by reference. The stacked layers could use junction-less transistors, recessed channel transistors, repeating layouts or other devices/techniques described in U.S. patent application Ser. No. 12/901,890 the content of which is incorporated by reference. The embodiments of this invention described in FIG. **14**-FIG. **21** may share a few common features. They can have multiple stacked (or overlying) layers, use one or more photodetector layers (terms photodetector layers and image sensor layers are often used interchangeably), thickness of at least one of the stacked layers is less than 5 microns and construction can be done with smart layer transfer techniques and stacking is done at temperatures approximately less than 450° C.

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In displays and microdisplays (small size displays where optical magnification is needed), transistors need to be formed on glass or plastic substrates. These substrates typically cannot withstand high process temperatures (e.g., >400° C.). Layer transfer can be advantageously used for constructing displays and microdisplays as well, since it may enable transistors to be processed on these substrates at <400° C. Various embodiments of transistors constructed on glass substrates are described in this patent application. These transistors constructed on glass substrates could form part of liquid crystal displays (LCDs) or other types of displays. It will be clear to those skilled in the art based on the present disclosure that these techniques can also be applied to plastic substrates.

FIGS. **22**A-G describe a process for forming recessed channel single crystal (or monocrystalline) transistors on glass substrates at a temperature approximately less than 400° C. for display and microdisplay applications. This process could include several steps that occur in a sequence from Step (A) to Step (G). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **22**A. A silicon wafer **2202** is taken and a n+ region **2204** is formed by ion implantation. Following this formation, a layer of p− Silicon **2206** is epitaxially grown. An oxide layer **2210** is then deposited. Following this deposition, an anneal is performed to activate dopants in various layers. It will be clear to one skilled in the art based on the present disclosure that various other procedures can be used to get the structure shown in FIG. **22**A.

Step (B) is illustrated in FIG. **22**B. Hydrogen is implanted into the structure shown in FIG. **22**A at a certain depth indicated by **2212**. Alternatively, Helium can be used for this purpose. Various elements in FIG. **22**B, such as **2202**, **2204**, **2006**, and **2210** have been described previously.

Step (C) is illustrated in FIG. **22**C. A glass substrate **2214** is taken and a silicon oxide layer **2216** is deposited atop it at compatible temperatures.

Step (D) is illustrated in FIG. **22**D. Various elements in FIG. **22**D, such as **2202**, **2204**, **2206**, **2210**, **2214**, and **2216** have been described previously. The structure shown in FIG. **22**B is flipped and bonded to the structure shown in FIG. **22**C using oxide-to-oxide bonding of layers **2210** and **2216**.

Step (E) is illustrated in FIG. **22**E. The structure shown in FIG. **22**D is cleaved at the hydrogen plane **2212** of FIG. **22**D. A CMP is then done to planarize the surface and yield the n+ Si layer **2218**. Various other elements in FIG. **22**E, such as **2214**, **2216**, **2210** and **2206** have been described previously.

Step (F) is illustrated in FIG. **22**F. Various elements in FIG. **22**F such as **2214**, **2216**, **2210**, and **2206** have been described previously. An oxide layer **2220** is formed using a shallow trench isolation (STI) process. This helps isolate transistors.

Step (G) is illustrated in FIG. **22**G. Various elements in FIG. **22**G such as **2210**, **2216**, **2220** and **2214** have been described previously. Using etch techniques, part of the n+ Silicon layer from FIG. **22**F and optionally p− Silicon layer from FIG. **22**F are etched. After this a thin gate dielectric is deposited, after which a gate dielectrode is deposited. The gate dielectric and gate electrode are then polished away to form the gate dielectric layer **2224** and gate electrode layer **2222**. The n+ Silicon layers **2228** and **2226** form the source and drain regions of the transistors while the p− Silicon region after this step is indicated by **2230**. Contacts and other parts of the display/microdisplay are then fabricated. It can be observed that during the whole process, the glass substrate substantially always experiences temperatures less than 400° C., or even lower. This is because the crystalline silicon can be transferred atop the glass substrate at a temperature less than 400° C., and dopants are pre-activated before layer transfer to glass.

FIG. **23**A-H describes a process of forming both nMOS and pMOS transistors with single-crystal silicon on a glass substrate at temperatures less than 400° C., and even lower. Ion-cut technology (which is a smart layer transfer technology) is used. While the process flow described is shown for both nMOS and pMOS on a glass substrate, it could also be used for just constructing nMOS devices or for just constructing pMOS devices. This process could include several steps that occur in a sequence from Step (A) to Step (H). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **23**A. A p− Silicon wafer **2302** is taken and a n well **2304** is formed on the p− Silicon wafer **2302**. Various additional implants to optimize dopant profiles can also be done. Following this formation, an isolation process is conducted to form isolation regions **2306**. A dummy gate dielectric **2310** made of silicon dioxide and a dummy gate electrode **2308** made of polysilicon are constructed.

Step (B) is illustrated in FIG. **23**B. Various elements of FIG. **23**B, such as **2302**, **2304**, **2306**, **2308** and **2310** have been described previously. Implants are done to form source-drain regions **2312** and **2314** for both nMOS and pMOS transistors. A rapid thermal anneal (RTA) is then done to activate dopants. Alternatively, a spike anneal or a laser anneal could be done.

Step (C) is illustrated in FIG. **23**C. Various elements of FIG. **23**C such as **2302**, **2304**, **2306**, **2308**, **2310**, **2312** and **2314** have been described previously. An oxide layer **2316** is deposited and planarized with CMP.

Step (D) is described in FIG. **23**D. Various elements of FIG. **23**D such as **2302**, **2304**, **2306**, **2308**, **2310**, **2312**, **2314**, and **2316** have been described previously. Hydrogen is implanted into the wafer at a certain depth indicated by **2318**. Alternatively, helium can be implanted.

Step (E) is illustrated in FIG. **23**E. Various elements of FIG. **23**E such as **2302**, **2304**, **2306**, **2308**, **2310**, **2312**, **2314**, **2316**, and **2318** have been described previously. Using a temporary bonding adhesive, the oxide layer is bonded to a temporary carrier wafer **2320**. An example of a temporary bonding adhesive is a polyimide that can be removed by shining a laser. An example of a temporary carrier wafer is glass.

Step (F) is described in FIG. **23**F. The structure shown in FIG. **23**E is cleaved at the hydrogen plane using a mechanical force. Alternatively, an anneal could be used. Following this cleave, a CMP is done to planarize the surface. An oxide layer is then deposited. FIG. **23**F shows the structure after all these steps are done, with the deposited oxide layer indicated as **2328**. After the cleave, the p− Silicon region is indicated as **2322**, the n− Silicon region is indicated as **2324**, and the oxide isolation regions are indicated as **2326**. Various other elements in FIG. **23**F such as **2308**, **2320**, **2312**, **2314**, **2310**, and **2316** have been described previously.

Step (G) is described in FIG. **23**G. The structure shown in FIG. **23**F is bonded to a glass substrate **2332** with an oxide layer **2330** using oxide-to-oxide bonding. Various elements in FIG. **23**G such as **2308**, **2326**, **2322**, **2324**, **2312**, **2314**, and **2310** have been described previously. Oxide regions **2328** and **2330** are bonded together. The temporary carrier wafer from FIG. **23**F is removed by shining a laser through it. A CMP process is then conducted to reach the surface of the gate electrode **2308**. The oxide layer remaining is denoted as **2334**.

Step (H) is described in FIG. **23**H. Various elements in FIG. **23**H such as **2312**, **2314**, **2328**, **2330**, **2332**, **2334**, **2326**, **2324**, and **2322** have been described previously. The dummy gate dielectric and dummy gate electrode are etched away in this step and a replacement gate dielectric **2336** and a replacement gate electrode **2338** are deposited and planarized with CMP. Examples of replacement gate dielectrics could be hafnium oxide or aluminum oxide while examples of replacement gate electrodes could be TiN or TaN or some other material. Contact formation, metallization and other steps for building a display/microdisplay are then conducted. It can be observed that after attachment to the glass substrate, no process step requires a processing temperature above 400° C.

FIGS. **24**A-F describe an embodiment of this invention, where single-crystal Silicon junction-less transistors are constructed above glass substrates at a temperature approximately less than 400° C. An ion-cut process (which is a smart layer transfer process) is utilized for this purpose. This process could include several steps that occur in a sequence from Step (A) to Step (F). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **24**A. A glass substrate **2402** is taken and a layer of silicon oxide **2404** is deposited on the glass substrate **2402**.

Step (B) is illustrated in FIG. **24**B. A p− Silicon wafer **2406** is implanted with a n+ Silicon layer **2408** above which an oxide layer **2410** is deposited. A RTA or spike anneal or laser anneal is conducted to activate dopants. Following this, hydrogen is implanted into the wafer at a certain depth indicated by **2412**. Alternatively, helium can be implanted.

Step (C) is illustrated in FIG. **24**C. The structure shown in FIG. **24**B is flipped and bonded onto the structure shown in FIG. **24**A using oxide-to-oxide bonding. This bonded structure is cleaved at its hydrogen plane, after which a CMP is done. FIG. **24**C shows the structure after all these processes are completed. **2414** indicates the n+ Si layer, while **2402**, **2404**, and **2410** have been described previously.

Step (D) is illustrated in FIG. **24**D. A lithography and etch process is conducted to pattern the n+ Silicon layer **2414** in FIG. **24**C to form n+ Silicon regions **2418** in FIG. **24**D. The glass substrate is indicated as **2402** and the bonded oxide layers **2404** and **2410** are shown as well.

Step (E) is illustrated in FIG. **24**E. A gate dielectric **2420** and gate electrode **2422** are deposited, following which a CMP is done. **2402** is as described previously. The n+ Si regions **2418** are not visible in this figure, since they are covered by the gate electrode **2422**. Oxide regions **2404** and **2410** have been described previously.

Step (F) is illustrated in FIG. **24**F. The gate dielectric **2420** and gate electrode **2422** from FIG. **24**E are patterned and etched to form the structure shown in FIG. **24**F. The gate dielectric after the etch process is indicated as **2424** while the gate electrode after the etch process is indicated as **2426**. n+ Si regions are indicated as **2418** while the glass substrate is indicated as **2402**. Oxide regions **2404** and **2410** have been described previously. It can be observed that a three-side gated junction-less transistor is formed at the end of the process described with respect of FIGS. **24**A-F. Contacts, metallization and other steps for constructing a display/microdisplay are performed after the steps indicated by FIGS.

24A-F. It can be seen that the glass substrate is not exposed to temperatures greater than approximately 400° C. during any step of the above process for forming the junction-less transistor.

FIGS. 25A-D describe an embodiment of this invention, where amorphous Si or polysilicon junction-less transistors are constructed above glass substrates at a temperature less than 400° C. This process could include several steps that occur in a sequence from Step (A) to Step (D). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. 25A. A glass substrate **2502** is taken and a layer of silicon oxide **2504** is deposited on the glass substrate **2502**. Following this deposition, a layer of n+ Si **2506** is deposited using low-pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). This layer of n+ Si could optionally be hydrogenated.

Step (B) is illustrated in FIG. 25B. A lithography and etch process is conducted to pattern the n+ Silicon layer **2506** in FIG. 25A to form n+ Silicon regions **2518** in FIG. 25B. **2502** and **2504** have been described previously.

Step (C) is illustrated in FIG. 25C. A gate dielectric **2520** and gate electrode **2522** are deposited, following which a CMP is optionally done. **2502** is as described previously. The n+ Si regions **2518** are not visible in this figure, since they are covered by the gate electrode **2522**.

Step (D) is illustrated in FIG. 25D. The gate dielectric **2520** and gate electrode **2522** from FIG. 25C are patterned and etched to form the structure shown in FIG. 25D. The gate dielectric after the etch process is indicated as **2524** while the gate electrode after the etch process is indicated as **2526**. n+ Si regions are indicated as **2518** while the glass substrate is indicated as **2502**. It can be observed that a three-side gated junction-less transistor is formed at the end of the process described with respect of FIGS. 25A-D. Contacts, metallization and other steps for constructing a display/microdisplay are performed after the steps indicated by FIGS. 25A-D. It can be seen that the glass substrate is not exposed to temperatures greater than 400° C. during any step of the above process for forming the junction-less transistor.

FIGS. 26A-C illustrate an embodiment of this invention, where a microdisplay is constructed using stacked RGB LEDs and control circuits are connected to each pixel with solder bumps. This process could include several steps that occur in a sequence from Step (A) to Step (C). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. 26A. Using procedures similar to FIG. 4A-S, the structure shown in FIG. 26A is constructed. Various elements of FIG. 26A are as follows:

2646—a glass substrate,

2644—an oxide layer, could be a conductive oxide such as ITO,

2634—an oxide layer, could be a conductive oxide such as ITO

2633—a an optional reflector, could be a Distributed Bragg Reflector or some other type of reflector,

2632—a P-type confinement layer that is used for a Blue LED (One example of a material for this region is GaN),

2630—a buffer layer that is typically used for a Blue LED (One example of a material for this region is AlGaN),

2628—a multiple quantum well used for a Blue LED (One example of materials for this region are InGaN/GaN),

2627—a N-type confinement layer that is used for a Blue LED (One example of a material for this region is GaN).

2648—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2622—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2621—an optional reflector (for example, a Distributed Bragg Reflector),

2620—a P-type confinement layer that is used for a Green LED (One example of a material for this region is GaN),

2618—a buffer layer that is typically used for a Green LED (One example of a material for this region is AlGaN),

2616—a multiple quantum well used for a Green LED (One example of materials for this region are InGaN/GaN),

2615—a N-type confinement layer that is used for a Green LED (One example of a material for this region is GaN),

2652—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2610—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2609—an optional reflector (for example, a Distributed Bragg Reflector),

2608—a P-type confinement layer used for a Red LED (One example of a material for this region is AlInGaP),

2606—a multiple quantum well used for a Red LED (One example of materials for this region are AlInGaP/GaInP),

2604—a P-type confinement layer used for a Red LED (One example of a material for this region is AlInGaP),

2656—an oxide layer, may be preferably a transparent conductive metal oxide such as ITO, and

2658—a reflector (for example, aluminum or silver).

Step (B) is illustrated in FIG. 26B. Via holes **2662** are etched to the substrate layer **2646** to isolate different pixels in the microdisplay/display. Also, via holes **2660** are etched to make contacts to various layers of the stack. These via holes may be preferably not filled. An alternative is to fill the via holes with a compatible oxide and planarize the surface with CMP. Various elements in FIG. 26B such as **2646**, **2644**, **2634**, **2633**, **2632**, **2630**, **2628**, **2627**, **2648**, **2622**, **2621**, **2620**, **2618**, **2616**, **2615**, **2652**, **2610**, **2609**, **2608**, **2606**, **2604**, **2656** and **2658** have been described previously.

Step (C) is illustrated in FIG. 26C. Using procedures similar to those described in respect to FIGS. 4A-S, the via holes **2660** have contacts **2664** (for example, with Aluminum) made to them. Also, using procedures similar to those described in FIGS. 4A-S, nickel layers **2666**, solder layers **2668**, and a silicon sub-mount **2670** with circuits integrated on them are constructed. The silicon sub-mount **2670** has transistors to control each pixel in the microdisplay/display. Various elements in FIG. 26C such as **2646**, **2644**, **2634**, **2633**, **2632**, **2630**, **2628**, **2627**, **2648**, **2622**, **2621**, **2620**, **2618**, **2616**, **2615**, **2652**, **2610**, **2609**, **2608**, **2606**, **2604**, **2656**, **2660**, **2662**, and **2658** have been described previously.

It can be seen that the structure shown in FIG. 26C can have each pixel emit a certain color of light by tuning the voltage given to the red, green and blue layers within each pixel. This microdisplay may be constructed using the ion-cut technology, a smart layer transfer technique.

FIGS. **27**A-D illustrate an embodiment of this invention, where a microdisplay is constructed using stacked RGB LEDs and control circuits are integrated with the RGB LED stack. This process could include several steps that occur in a sequence from Step (A) to Step (D). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **27**A. Using procedures similar to those illustrated in FIGS. **4**A-S, the structure shown in FIG. **27**A is constructed. Various elements of FIG. **27**A are as follows:

2746—a glass substrate,

2744—an oxide layer, could be a conductive oxide such as ITO,

2734—an oxide layer, could be a conductive oxide such as ITO,

2733—a an optional reflector (e.g., a Distributed Bragg Reflector or some other type of reflector),

2732—a P-type confinement layer that is used for a Blue LED (One example of a material for this region is GaN),

2730—a buffer layer that is typically used for a Blue LED (One example of a material for this region is AlGaN),

2728—a multiple quantum well used for a Blue LED (One example of materials for this region are InGaN/GaN),

2727—a N-type confinement layer that is used for a Blue LED (One example of a material for this region is GaN),

2748—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2722—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2721—an optional reflector (e.g., a Distributed Bragg Reflector),

2720—a P-type confinement layer that is used for a Green LED (One example of a material for this region is GaN),

2718—a buffer layer that is typically used for a Green LED (One example of a material for this region is AlGaN),

2716—a multiple quantum well used for a Green LED (One example of materials for this region are InGaN/GaN),

2715—a N-type confinement layer that is used for a Green LED (One example of a material for this region is GaN),

2752—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2710—an oxide layer, may be preferably a conductive metal oxide such as ITO,

2709—an optional reflector (e.g., a Distributed Bragg Reflector),

2708—a P-type confinement layer used for a Red LED (One example of a material for this region is AlInGaP),

2706—a multiple quantum well used for a Red LED (One example of materials for this region are AlInGaP/GaInP),

2704—a P-type confinement layer used for a Red LED (One example of a material for this region is AlInGaP),

2756—an oxide layer, may be preferably a transparent conductive metal oxide such as ITO,

2758—a reflector (e.g., aluminum or silver).

Step (B) is illustrated in FIG. **27**B. Via holes **2762** are etched to the substrate layer **2746** to isolate different pixels in the microdisplay/display. Also, via holes **2760** are etched to make contacts to various layers of the stack. These via holes may be preferably filled with a compatible oxide and the surface can be planarized with CMP. Various elements of FIG. **27**B such as **2746**, **2744**, **2734**, **2733**, **2732**, **2730**, **2728**, **2727**, **2748**, **2722**, **2721**, **2720**, **2718**, **2716**, **2715**, **2752**, **2710**, **2709**, **2708**, **2706**, **2704**, **2756** and **2758** have been described previously.

Step (C) is illustrated in FIG. **27**C. Metal **2764** (for example) is constructed within the via holes **2760** using procedures similar to those described in respect to FIGS. **4**A-S. Following this construction, an oxide layer **2766** is deposited. Various elements of FIG. **27**C such as **2746**, **2744**, **2734**, **2733**, **2732**, **2730**, **2728**, **2727**, **2748**, **2722**, **2721**, **2720**, **2718**, **2716**, **2715**, **2752**, **2710**, **2709**, **2708**, **2706**, **2704**, **2756**, **2760**, **2762** and **2758** have been described previously.

Step (D) is illustrated in FIG. **27**D. Using procedures described in co-pending U.S. patent application Ser. No. 12/901,890, the content of which is incorporated herein by reference, a single crystal silicon transistor layer **2768** can be monolithically integrated using ion-cut technology atop the structure shown in FIG. **27**C. This transistor layer **2768** is connected to various contacts of the stacked LED layers (not shown in the figure for simplicity). Following this connection, nickel layer **2770** is constructed and solder layer **2772** is constructed. The packaging process then is conducted where the structure shown in FIG. **27**D is connected to a silicon sub-mount.

It can be seen that the structure shown in FIG. **27**D can have each pixel emit a certain color of light by tuning the voltage given to the red, green and blue layers within each pixel. This microdisplay is constructed using the ion-cut technology, a smart layer transfer technique. This process where transistors are integrated monolithically atop the stacked RGB display can be applied to the LED concepts disclosed in association with FIGS. **4-10**.

The embodiments of this invention described in FIGS. **26-27** may enable novel implementations of "smart-lighting concepts" (also known as visible light communications) that are described in "Switching LEDs on and off to enlighten wireless communications", EETimes, June 2010 by R. Colin Johnson. For these prior art smart lighting concepts, LED lights could be turned on and off faster than the eye can react, so signaling or communication of information with these LED lights is possible. An embodiment of this invention involves designing the displays/microdisplays described in FIGS. **26-27** to transmit information, by modulating wavelength of each pixel and frequency of switching each pixel on or off. One could thus transmit a high bandwidth through the visible light communication link compared to a LED, since each pixel could emit its own information stream, compared to just one information stream for a standard LED. The stacked RGB LED embodiment described in FIGS. **4**A-S could also provide a improved smart-light than prior art since it allows wavelength tunability besides the ability to turn the LED on and off faster than the eye can react.

NuSolar Technology:

Multijunction solar cells are constructed of multiple p-n junctions stacked atop each other. Multi-junction solar cells are often constructed today as shown in FIG. **18**A. A Germanium substrate **2800** is taken and multiple layers are grown epitaxially atop it. The first epitaxial layer is a p-type doped Ge back-surface field (BSF) layer, indicated as **2802**. Above it, a n-type doped Ge base layer **2804** is epitaxially grown. A InGaP hetero layer **2806** is grown above this. Following this growth, a n-type InGaAs buffer layer **2808** is grown. A tunnel junction **2810** is grown atop it. The layers **2802**, **2804**, **2806**, and **2808** form the bottom Ge cell **2838** of the multi-junction solar cell described in FIG. **18**A. Above this bottom cell and the tunnel junction **2810**, a middle cell constructed of InGaAs is epitaxially grown, and is indicated as **2836**. The InGaAs middle cell has the following 4 layers: a p+ doped back surface field (BSF) layer **2812** of InGaP, a p doped base layer **2814** of InGaAs, a n doped emitter layer **2816** of InGaAs, and a n+ doped window layer **2818** of InGaP. Above this InGaAs middle cell **2836**, a tunnel junction **2820** is grown epitaxially and above this, another cell, constructed of InGaP, and called a top cell **2834** is epitaxially grown. This top cell **2834** has the following layers: a p+ doped back-surface field (BSF) layer of AlInGaP **2822**, a p doped base layer of InGaP **2824**, a n doped emitter layer of InGaP **2826** and a n+ doped window layer of AlInP **2828**. Above this layer of AlInP **2828**, a GaAs layer **2830** is epitaxially grown, Aluminum contacts **2840** are deposited and an anti-reflection (AR) coating **2832** is formed. The purpose of back-surface field (BSF) layers in the multi-junction solar cell depicted in FIG. **18**A is to reduce scattering of carriers towards the tunnel junctions. The purpose of the window layers is to reduce surface recombination velocity. Both the BSF layers and window layers are heterojunctions that help achieve the above mentioned purposes. Tunnel junctions help achieve good ohmic contact between various junctions in the multi-junction cell. It can be observed that the bottom, middle and top cells in the multi-junction cell are arranged in the order of increasing band-gap and help capture different wavelengths of the sun's spectrum.

FIG. **28**B shows the power spectrum of the sun vs. photon energy. It can be seen that the sun's radiation has energies in between 0.6 eV and 3.5 eV. Unfortunately though, the multi-junction solar cell shown in FIG. **28**A has band-gaps not covering the solar spectrum (band-gap of cells varies from 0.65 eV to 1.86 eV).

FIG. **28**C shows the solar spectrum and indicates the fraction of solar power converted to electricity by the multi-junction solar cell from FIG. **28**A. It can be observed from FIG. **28**C that a good portion of the solar spectrum is not converted to electricity. This is largely because the band-gap of various cells of the multi-junction solar cell does not cover the entire solar spectrum.

FIGS. **29**A-H show a process flow for constructing multi-junction solar cells using a layer transfer flow. Although FIGS. **29**A-H show a process flow for stacking two cells with two different bandgaps, it is fairly general, and can be extended to processes involving more than two cells as well. This process could include several steps that occur in a sequence from Step (A) to Step (H). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **29**A. Three wafers **2920**, **2940** and **2946** have different materials grown or deposited above them. Materials from these three wafers **2920**, **2940** and **2946** are stacked using layer transfer to construct the multi-junction solar cell described in this embodiment of the invention. The wafer **2946** includes a substrate C denoted as **2942** above which an oxide layer C, denoted as **2944**, is deposited. Examples of materials for **2942** include heavily doped silicon and the oxide layer C **2944** could preferably be a conductive metal oxide such as ITO. The wafer **2940** includes a substrate for material system B, also called substrate B **2938** (e.g., InP or GaAs), a buffer layer **2936**, a p++ contact layer B (e.g., InGaP) **2934**, a p+ back-surface field (BSF) layer B (e.g., InGaP) **2932**, a p base layer B (eg. InGaAs) **2930**, a n emitter layer B (e.g., InGaAs) **2928**, a n+ window layer B (e.g., InGaP) **2926**, a n++ contact layer B (e.g., InGaP) **2924** and an oxide layer B (e.g., ITO) **2922**. The wafer **2920** includes a substrate for material system A, also called substrate A **2918** (e.g., InP or GaAs), a buffer layer **2916**, a p++ contact layer A (eg. AlInGaP) **2914**, a p+ back-surface field (BSF) layer A (e.g., AlInGaP) **2912**, a p-base layer A (e.g., InGaP) **2910**, a n-emitter layer A (e.g., InGaP) **2918**, a n+ window layer A (e.g., AlInP) **2916**, a n++ contact layer A (e.g., AlInP) **2914** and an oxide layer A (e.g., ITO) **2912**. Various other materials and material systems can be used instead of the examples of materials listed above.

Step (B) is illustrated in FIG. **29**B. Hydrogen is implanted into the structure **2920** of FIG. **29**A at a certain depth indicated by **2948**. Various other elements of FIG. **29**B such as **2902**, **2904**, **2906**, **2908**, **2910**, **2912**, **2914**, **2916**, and **2918** have been described previously. Alternatively, Helium can be implanted instead of hydrogen. Various other atomic species can be implanted.

Step (C) is illustrated in FIG. **29**C. The structure shown in FIG. **29**B is flipped and bonded atop the structure indicated as **2946** in FIG. **29**A. Various elements in FIG. **29**C such as **2902**, **2904**, **2906**, **2908**, **2910**, **2912**, **2914**, **2916**, **2944**, **2942**, and **2918** have been described previously.

Step (D) is illustrated in FIG. **29**D. The structure shown in FIG. **29**C may be cleaved at its hydrogen plane **2948** preferably using a sideways mechanical force. Alternatively, an anneal could be used. A CMP is then done to planarize the surface to produce p++ contact layer A **2915**. Various other elements in FIG. **29**D such as **2942**, **2944**, **2902**, **2904**, **2906**, **2908**, **2910**, and **2912** have been described previously. The substrate **2918** from FIG. **29**C removed by cleaving may be reused.

Step (E) is illustrated in FIG. **29**E. An oxide layer **2950** is deposited atop the structure shown in FIG. **29**D. This oxide layer **2950** may be preferably a conductive metal oxide such as ITO, although an insulating oxide could also be used. Various elements in FIG. **29**E such as **2942**, **2944**, **2902**, **2904**, **2906**, **2908**, **2910**, **2915**, and **2912** have been described previously.

Step (F) is illustrated using FIG. **29**F. The structure indicated as **2940** in FIG. **29**A is implanted with hydrogen at a certain depth **2952**. Alternatively, Helium or some other atomic species can be used. Various elements of FIG. **29**F such as **2922**, **2924**, **2926**, **2928**, **2930**, **2932**, **2934**, **2936**, and **2938** have been indicated previously.

Step (G) is illustrated in FIG. **29**G. The structure shown in FIG. **29**F is flipped and bonded onto the structure shown in FIG. **29**E using oxide-to-oxide bonding. Various elements in FIG. **29**G such as **2942**, **2944**, **2902**, **2904**, **2906**, **2908**, **2910**, **2912**, **2915**, **2950**, **2922**, **2924**, **2926**, **2928**, **2930**, **2932**, **2934**, **2936**, **2952**, and **2938** have been indicated previously.

Step (H) is illustrated in FIG. **29**H. The structure shown in FIG. **29**G is cleaved at its hydrogen plane **2952**. A CMP is then done to planarize the surface and produces the p++ contact layer B indicated as **2935** in FIG. **29**H. Above this, an oxide layer **2952** (e.g., ITO) is deposited. The substrate B indicated as **2938** in FIG. **29**G can be reused after cleave. Various other elements in FIG. **29**H such as **2942**, **2944**, **2902**, **2904**, **2906**, **2908**, **2910**, **2912**, **2915**, **2950**, **2922**, **2924**, **2926**, **2928**, **2930**, and **2932** have been indicated previously.

After completing steps (A) to (H), contacts and packaging are then done. One could make contacts to the top and bottom of the stack shown in FIG. **29**H using one front contact to ITO layer **2954** and one back contact to the heavily doped Si substrate **2942**. Alternatively, contacts could be made to each cell of the stack shown in FIG. **29**H as described in respect to

FIG. **4**A-S. While FIGS. **29**A-H show two cells in series for the multijunction solar cell, the steps shown in the above description can be repeated for stacking more cells that could be constructed of various band gaps. The advantage of the process shown in FIG. **29**A-H is that all processes for stacking are done at temperatures less than 400° C., and could even be done at less than 250° C. Therefore, thermal expansion co-efficient mismatch may be substantially mitigated. Likewise, lattice mismatch may be substantially mitigated as well. Therefore, various materials such as GaN, Ge, InGaP and others which have widely different thermal expansion co-efficients and lattice constant can be stacked atop each other. This flexibility in use of different materials may enable a full spectrum solar cell or a solar cell that covers a increased band within the solar spectrum than the prior art cell shown in FIG. **28**A.

FIGS. **30**A-D show a process flow for constructing another embodiment of this invention, a multi-junction solar cell using a smart layer transfer technique (ion-cut). This process may include several steps that occur in a sequence from Step (A) to Step (D). Many of these steps share common characteristics, features, modes of operation, etc. When identical reference numbers are used in different drawing figures, they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

Step (A) is illustrated in FIG. **30**A. It shows a multi-junction solar cell constructed using epitaxial growth on a heavily doped Ge substrate, as described in the prior art multi-junction solar cell of FIG. **28**A. The structure shown in FIG. **30**A includes the following components:

3002—a Ge substrate,
3004—a p-type Ge BSF layer,
3006—a n-type Ge base layer,
3008—a InGaP hetero layer,
3010—a n-type InGaAs buffer layer,
3012—a tunnel junction,
3014—a p+ InGaP BSF layer,
3016—a p-type InGaAs base layer,
3018—a n-type InGaAs emitter layer,
3020—a n+ InGaP window layer,
3022—a tunnel junction,
3024—a p+ AlInGaP BSF layer,
3026—a p-type InGaP BSF layer,
3028—a n-type InGaP emitter layer,
3030—a n+-type AlInP window layer, and
3032—an oxide layer, may be preferably of a conductive metal oxide such as ITO. Further details of each of these layers is provided in the description of FIG. **28**A.

Step (B) is illustrated in FIG. **30**B. Above a sapphire or SiC or bulk GaN substrate **3034**, various layers such as buffer layer **3036**, a n+ GaN layer **3038**, a n InGaN layer **3040**, a p-type InGaN layer **3042** and a p+ GaN layer **3044** are epitaxially grown. Following this growth, an oxide layer **3046** may be constructed preferably of a transparent conducting oxide such as, for example, ITO is deposited. Hydrogen is implanted into this structure at a certain depth indicated as **3048**. Alternatively, Helium or some other atomic species can be implanted.

Step (C) is illustrated in FIG. **30**C. The structure shown in FIG. **30**B is flipped and bonded atop the structure shown in FIG. **30**A using oxide-to-oxide bonding. Various elements in FIG. **30**C such as **3002**, **3004**, **3006**, **3008**, **3010**, **3012**, **3014**, **3016**, **3018**, **3020**, **3022**, **3024**, **3026**, **3028**, **3030**, **3032**, **3048**, **3046**, **3044**, **3042**, **3040**, **3038**, **3036**, and **3034** have been described previously.

Step (D) is illustrated using FIG. **30**D. The structure shown in FIG. **30**C is cleaved at its hydrogen plane **3048**. A CMP process is then conducted to result in the n+ GaN layer **3041**. Various elements in FIG. **30**D such as **3002**, **3004**, **3006**, **3008**, **3010**, **3012**, **3014**, **3016**, **3018**, **3020**, **3022**, **3024**, **3026**, **3028**, **3030**, **3032**, **3046**, **3044**, **3042**, and **3038** have been described previously.

After completing steps (A) to (D), contacts and packaging are then done. Contacts may be made to the top and bottom of the stack shown in FIG. **30**D, for example, one front contact to the n+ GaN layer **3041** and one back contact to the heavily doped Ge substrate **3002**. Alternatively, contacts could be made to each cell of the stack shown in FIG. **30**D as described in FIGS. **4**A-S.

FIGS. **29-30** described solar cells with layer transfer processes. Although not shown in FIG. **29-30**, it will be clear to those skilled in the art based on the present disclosure that front and back reflectors could be used to increase optical path length of the solar cell and harness more energy. Various other light-trapping approaches could be utilized to boost efficiency as well.

An aspect of various embodiments of this invention is the ability to cleave wafers and bond wafers at lower temperatures (e.g., less than 400° C. or even less than 250° C.). In co-pending U.S. patent application Ser. No. 12/901,890 the content of which is incorporated by reference, several techniques to reduce temperatures for cleave and bond processes are described. These techniques are herein incorporated in this document by reference.

Several material systems have been quoted as examples for various embodiments of this invention in this patent application. It will be clear to one skilled in the art based on the present disclosure that various other material systems and configurations can also be used without violating the concepts described. It will also be appreciated by persons of ordinary skill in the art that the present invention is not limited to what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and sub-combinations of the various features described hereinabove as well as modifications and variations which would occur to such skilled persons upon reading the foregoing description. Thus the invention is to be limited only by the appended claims.

We claim:

1. An integrated device, comprising:
an image sensor array and an image circuit array;
wherein said image sensor array comprises a first mono-crystallized silicon layer, and said image circuit array comprises a second mono-crystallized silicon layer,
wherein disposed between said first mono-crystallized silicon layer and said second mono-crystallized silicon layer is thin isolation layer, and
wherein said first mono-crystallized silicon layer or said second mono-crystallized silicon layer thickness is less than 400 nm, and
wherein said second mono-crystal layer comprises a plurality of single crystal transistors,
wherein said image sensor array comprises a plurality of image sensor pixels,
wherein said image sensor pixels and said single crystal transistors are aligned to each other.

2. An integrated device according to claim **1**,
wherein said second mono-crystal layer is less than 2 microns thick.

3. An integrated device according to claim 1,

wherein said first mono-crystallized silicon layer comprises two crystalline layers,

wherein said two crystalline layers comprise a first image sensor layer and a second image sensor layer, and

wherein said first image sensor layer is sensitive to a different spectrum than said second image sensor layer.

4. An integrated device, comprising:

an image sensor array and an image circuit array;

wherein said image sensor array comprises a first mono-crystallized silicon layer, and said image circuit array comprises a second mono-crystallized silicon layer,

wherein disposed between said first mono-crystallized silicon layer and said second mono-crystallized silicon layer is thin isolation layer, and

wherein said first mono-crystallized silicon layer or said second mono-crystallized silicon layer thickness is less than 400 nm, and

wherein said second mono-crystal layer comprises a plurality of single crystal transistors,

wherein said second mono-crystal layer comprises two crystalline layers,

wherein said two crystalline layers comprise a first transistors layer and a second transistors layer.

5. An integrated device according to claim 4,

wherein said first mono-crystallized silicon layer comprises two crystalline layers,

wherein said two crystalline layers comprise a first image sensor layer and a second image sensor layer, and

wherein at least one of said two crystalline layers is less than 2 microns thick.

6. An integrated device according to claim 4,

wherein said single crystal transistors form a plurality of pixel control circuits.

7. An integrated device, comprising:

an image sensor array and an image circuit array;

wherein said image sensor array comprises a first mono-crystallized silicon layer, and said image circuit array comprises a second mono-crystallized silicon layer,

wherein disposed between said first mono-crystallized silicon layer and said second mono-crystallized silicon layer is a thin isolation layer,

wherein said first mono-crystallized silicon layer or said second mono-crystallized silicon layer thickness is less than 400 nm, and

wherein through said thin isolation layer are a multiplicity of conducting vias, and

wherein said conducting vias have a diameter of less than 200 nm, and

a third mono-crystallized silicon layer underlying said second mono-crystallized silicon layer,

wherein said third mono-crystallized silicon layer comprises pixel electronics read-out and control circuits.

8. An integrated device according to claim 7,

wherein said image sensor array is bonded on top of said image circuit array forming two substantially parallel planes, and

wherein said bonded leaves a re-useable base wafer used to hold said mono-crystallized silicon layer.

9. An integrated device according to claim 7,

wherein said image sensor array comprises a first image sensor array and a second image sensor array, and

wherein said first image sensor array optical sensitivity is substantially different than said second image sensor array.

10. An integrated device according to claim 7,

wherein said second mono-crystalline silicon layer comprises a plurality of single crystal transistors, and

wherein said single crystal transistors form a plurality of pixel control circuits.

11. An integrated device according to claim 7,

wherein said second mono-crystallized silicon layer comprises an infra-red photo detector.

12. An integrated device, comprising:

an image sensor array and an image circuit array;

wherein said image sensor array comprises a first mono-crystallized silicon layer, and said image circuit array comprises a second mono-crystallized silicon layer,

wherein disposed between said first mono-crystallized silicon layer and said second mono-crystallized silicon layer is thin isolation layer, and

wherein said first mono-crystallized silicon layer or said second mono-crystallized silicon layer thickness is less than 400 nm, and

a third mono-crystallized silicon layer underlying said first mono-crystallized silicon layer,

wherein said third mono-crystallized silicon layer comprises pixel electronics read-out and control circuits.

13. An integrated device according to claim 12,

wherein said image sensor array is bonded on top of said image circuit array forming two substantially parallel planes, and

wherein said bonded leaves a re-useable base wafer used to hold said mono-crystallized silicon layer.

14. An integrated device according to claim 12,

wherein said image sensor array comprises a first image sensor array and a second image sensor array, and

wherein said first image sensor array optical sensitivity is substantially different than said second image sensor array.

15. An integrated device according to claim 12, further comprising:

a multiplicity of through silicon layer conducting vias,

wherein said conducting vias have a diameter of less than 200 nm.

16. An integrated device according to claim 12,

wherein said second mono-crystallized silicon layer comprises an infra-red photo detector.

17. An integrated device according to claim 12,

wherein said image sensor array comprises a first image sensor array and a second image sensor array, and

wherein disposed between said first image sensor array and said second image sensor array is a wire grid polarizer.

18. An integrated device according to claim 1,

wherein said single crystal transistors form a plurality of pixel control circuits.

19. An integrated device according to claim 4,

wherein said first mono-crystallized silicon layer comprises two crystalline layers,

wherein said two crystalline layers comprise a first image sensor layer and a second image sensor layer, and

wherein said first image sensor layer is sensitive to a different spectrum than said second image sensor layer.

20. An integrated device according to claim 7,

wherein said first mono-crystallized silicon layer comprises two crystalline layers,

wherein said two crystalline layers comprise a first image sensor layer and a second image sensor layer, and

wherein said first image sensor layer is sensitive to a different spectrum than said second image sensor layer.

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